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## **Packaging process development for visible LEDs**

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<p>Valoa emittoivien diodien (LED) pakkausprosessi on suurin kuluerä koko tuotannossa. Tämä hidastaa korkean hyötysuhteen LED:ien laajaa omaksumista yleisvalaistukseen. Tässä diplomityössä kehitettiin pakkausprosessi optisen alueen LED:lle. Tutkimus ja kehitys suoritettiin Aalto-yliopiston Optoelektroniikan tutkimusryhmässä. Pakattujen LED:ien suorituskkyä tutkittiin elektroluminesenssi-mittauksilla ja pakkausepoksia optisella transmissiomittauksella.</p> <p>Kehitetty pakkausprosessi koostuu neljästä päävaiheesta. Ensin prosessoitu safiirikiekko sahataan yksittäisiksi LED-siruiksi kiekkosahalla. Seuraavaksi LED-siru kiinnitetään metalliseen kahden pinnan TO-46 alustaan kiinnitysepoksilla. Tämän jälkeen sirun sähköiset kontaktit liitetään alumiinilangalla metallialustan kontakteihin. Lopulta LED-komponentti koteloidaan valamalla se läpinäkyvään pakkausepoksiin. Työn tuloksena valmistettiin sinisiä matalateho-LED:ejä tutkimustarkoituksiin.</p> <p>Mittausten tuloksena todettiin valitun kupuepoksen pystyvän korkeaan transmissioon sinisten LED:ien emissioaallonpituudella ja koko näkyvällä alueella. Elektroluminesenssimittausten tuloksena puolestaan havaittiin pakkausprosessoitujen LED:ien pystyvän tuottamaan 5,3 % ulkoisen kvanttihyötysuhteen (EQE, external quantum efficiency) ja 3,5 mW optisen tehon 20 mA ajovirralla. Optista suorituskkyä mitattiin ja vertailtiin myös prosessoidun kiekon kolmen eri alueen LED-siruihin ennen ja jälkeen epoksikoteloinnin. Mittaukset osoittivat LED-kiekolla esiintyvän eroja LED:ien optisessa tehossa ja EQE:ssä. Lisäksi epoksin todettiin laskevan emittoituvaa optista tehoa. Silti pakkausprosessin laadun todettiin täyttävän LED-pakkauksen vaatimukset riittävästi.</p>		
Avainsanat: LED, pakkaus, back-end -prosessi, kiekkosahaus, sirukiinnitys, lanka-bondaus, epoksi, elektroluminesenssi		



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<p>The back-end processing of light-emitting diode (LED) lighting incurs the highest cost quantity for the whole production. This hinders the adoption of highly efficient LEDs. In this work a packaging process for visible LEDs was developed. The research and development was carried out at the Optoelectronics research group of Aalto University. The performance of the packaged LEDs was studied by electroluminescence (EL) measurements and the encapsulation epoxy with optical transmission measurements.</p> <p>The packaging process consisted of four main stages. First, the singulation of the processed sapphire wafer into chips was performed with a blade-based dicing machine. Second, the LED chip was bonded with attachment epoxy onto a TO-46 two-pin metallic header. Third, wire-bonding was performed by an aluminum bond wire from the chip contacts to the header contacts. Finally, encapsulation was carried out with a transparent packaging epoxy. As a result, in-house fabricated blue LED devices operating on 20 mA drive current were produced for research purposes.</p> <p>It was observed with absolute irradiance measurements that the back-end processed LEDs can provide external quantum efficiencies (EQE) of 5,3 % and of 3,5 mW optical output powers with a 20 mA current. Furthermore, the studies of the used epoxy showed a high transmission for the average operation wavelength of the used LEDs. Also, the uniformity of the performance metrics of a processed LED wafer was tested by packaging and characterizing LEDs at three different wafer locations before and after encapsulation. Results showed that there were slight on-wafer performance variations regarding the optical power and the EQE. Moreover, optical power degradation was observed after encapsulation.</p>		
Keywords: LED, packaging, back-end-processing, dicing, chip attachment, wire-bonding, epoxy encapsulation, electroluminescence		

## Preface

This Master's thesis was conducted at the Aalto University, School of Electrical Engineering, Optoelectronics research group. I want to express my utmost gratitude to the thesis supervisor Professor Markku Sopanen who made this work possible by allowing me to work among this project in Micronova and for possibility to prolong its completion. I also want to thank my thesis adviser M.Sc. Lauri Riuttanen for his expertise, patience and effort for completion of this thesis. Also, I express thanks to Lauri for our non-work related discussions, mainly on Elder's Scroll V: Skyrim, which gave me a much needed break from the world of back-end processing.

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*∴..the living throne, the sapphire-blaze, where angels tremble while they gaze, he saw,  
but blasted with excess of light, closed his eyes in endless night."*

-Thomas Gray

Otaniemi, 10.3.2014

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# Abbreviations

## Abbreviations

AFM	Atomic Force Microscopy
CBN	Cubic Boron Nitride
CCD	Charge Coupled Device
CER	Cycloaliphatic Epoxy Resin
CL	Cathodoluminescence
CSL	Current Spreading Layer
CTE	Coefficient of Thermal Expansion
DAF	Die Attach Film
DC	Direct Current
DGEBA	Diglycidyl Ether (of) Bisphenol A
DRIE	Deep Reactive Ion Etching
EBL	Electron Blocking Layer
EFO	Electronic Flame Off
EL	Electroluminescence
FR-4	Flame Resistant 4 (breadboard)
GaN	Gallium Nitride
HBLED	High-Brightness Light-Emitting Diode
HHPA	Hexahydrophtalic Anhydride
HPLED	High-Power Light-Emitting Diode
ICP-RIE	Inductively Coupled Plasma Reactive Ion Etching
IPA	Isopropanol Alcohol
IQE	Internal Quantum Efficiency
IR	Infrared
ITO	Indium Tin Oxide
LED	Light-Emitting Diode
MBE	Molecular Beam Epitaxy
MEMS	Micro-Electro-Mechanical-System
MOVPE	Metalorganic Vapor Phase Epitaxy
MQW	Multiple Quantum Well
PL	Photoluminescence
POM	Polyoxymethylene
QW	Quantum Well
RGB	Red, Green, Blue
RPM	Rotation Per Minute
RTV	Room Temperature Vulcanizing
SRH	Shockley-Read-Hall
TO-46	Transistor-Outline 46
TSV	Through Silicon Via
US	Ultrasonic
WPE	Wall-Plug-Efficiency
XRD	X-Ray Diffraction

# 1 Introduction

Currently, solid-state lighting is a strongly emerging commercial semiconductor technology branch. The commercial spearhead-product of solid-state lighting technology is the light-emitting diode (LED) that represents a multi-billion dollar global business [1]. LEDs offer the promise of the highest illumination efficiency ever produced. Nowadays, LEDs are mainly used for high-end applications such as displays, mobile phones and on car headlights. Nevertheless, it has been predicted that as the euro-per-lumen ratio of LED's is further reduced, incandescent light bulbs and fluorescent lamps will become obsolete and thus lead to a massive adoption of LEDs for general lighting [1]. The key for further price reduction and efficiency increase lie especially with the back-end processing of LED devices.

In order to obtain an operating semiconductor device after its front-end fabrication, it has to be singulated to chips, packaged, electrically connected and properly protected. These post-microfabrication processing steps are called back-end or packaging process. In general, the back-end processing is responsible for the largest cost quantity in semiconductor device production and has thus increasing importance due to the constant desire to cut the cost of production. Besides these commercial benefits, back-end processing development also provides a wide and important platform for overall device efficiency and performance improvements. [2] These aspects are especially pronounced in the case of solid-state devices on which the optical transmission properties of encapsulation material are of a paramount importance. Tackling these kinds of material and process issues is also a core reason for this work.

In this master's thesis, a visible domain LED packaging process development and processing for research purposes were designed and described. This work was conducted in the Aalto university at Micronova research center. The optoelectronic research group produced the front-end processed LEDs.

The front-end processed outset-LEDs were in-house produced, blue-light emitting, gallium nitride (GaN) based LED-wafers. The developed process starts from a protective resist spinning on top of the processed sapphire wafer followed by dicing into individual chips. Then, the resist is removed on chip level and a consecutive microscopy and probe-station functionality testing are performed. After that, the functional LED chips are attached to metal headers using thermally and electrically conductive epoxy. This attachment is followed by a wedge-wedge wire bonding process from the chip to the header contact pads in order to ensure an electrical path through the structure. After the second functionality testing, the LED component is incased by encapsulation epoxy in a dome-shaped silicone mold. Lastly, these packaged components were end-tested. This developed process was demonstrated to be able to deliver high yield and repeatability. As a part of performance testing, the optical output-power, external quantum efficiency (EQE) and transmission measurements for encapsulation epoxy were conducted on some samples by using electroluminescence (EL) measurements.

Regarding the topical scope, this master's thesis is not meant to be a comprehensive description of modern industrial or experimental LED packaging process', nor is this work going to depict more challenging high-power LED packaging or electricity converting circuitry issues. Additional processing from a simple, packaged LED component, such as circuit, module and lamp level schemes, are out of the scope of this master's thesis. Still, a flip-chip back-end processing technology, white light emitting LEDs and thermal energy management issues are shortly addressed due to their importance in contemporary LED production and as potential follow-up development topics.

After this introductory chapter, the thesis structure is as follows. Chapter 2 presents the theoretical and general background of the LED packaging processes together with a short LED physics summary. Chapter 3 discusses the actual developed packaging process with detailed process flows in appendices's. Chapter 4 depicts the LED characterization schemes and used measurement setups. Chapter 5 discusses the obtained results. Finally, chapter 6 concludes and summarize the thesis.

## 2 Background

### 2.1 LED Technology

Light-emitting diodes, (LEDs), are strongly emerging technology in lighting markets due to their increasing light efficiency, long life time and decreasing prices. LEDs are currently a major business and it is predicted that a massive general lighting market adoption will occur when the production efficiency and performance of the LEDs keep on improving. The back-end processing of LEDs corresponds the biggest cost quantity, while the substrate, material and front-end processing costs are smaller due to the benefits of large scale batch fabrication. For LEDs, the biggest lighting market sector in terms of revenue per application is general lighting followed by LED based displays. LEDs are also currently used in cell phones, automotive industry products, projectors and laptops. [1]

Light generation in LEDs is based on radiative electron-hole recombination in a pn-junction consisting of doped semiconductor compounds. In general, the grand technological value of semiconductors stems from the versatile and tunable electrical and optical properties of the materials. These properties are tailorable due to the existence of energy stage bands which arises from the crystal structure geometry of a given semiconductor. Thus, in crystalline solid-state materials, energy states of charge carriers are divided on semi-continuous bands of which the most relevant for light emission are the conduction band and the valence band. More specifically, the valence band is defined to be the highest fully occupied band at absolute zero temperature while the conduction band is the lowest empty band at 0 K. Semiconductors are materials for which the forbidden energy gap (*i.e.*, valence-conduction band energy separation) is typically between 0 and 3 eV. Still, this definition should not been seen as a strict range because sometimes even larger band gap materials are called semiconductors in literature. [3] The band structure of given semiconductor can be determined from the Schrödinger equation by using certain approximations on the potential energy. [4] A good review on such energy band calculations on solid semiconductors can be found in Ref. 3.

The occupation of energy states structure on the vicinity of the band gap determines the degree of conduction of a given semiconductor. At absolute zero temperature, occupation of electrons extends to so called Fermi energy, which in the case of semiconductors is inside the forbidden energy gap. Therefore intrinsic semiconductors are usually slightly conducting at room temperature due to a minor conduction band occupation of thermally excited electrons. The versatility of semiconductors is achieved through the ability to alter the resistivity of semiconductors by an addition of appropriate impurity atoms. These impurity atoms can function as acceptors, which render an intrinsic semiconductor p-type by producing additional holes (*i.e.*, unoccupied states) into the valence band. Respectively, donors can make intrinsic semiconductor n-type by addition of electrons to the conduction band.

In general, the electric behavior of semiconductor structures can be controlled by applying a voltage over the structure. In the case of LEDs, the diode junction is excited by forward biasing. This causes an electric current through the LED and electrons start to recombine with holes. This occurs effectively in the depletion zone within the pn-junction area of the LED including typically quantum well(s) (QWs). The QWs greatly improve the overall radiative recombination efficiency. The light is thus produced when the recombining electrons and holes emit the energy difference as photons. This takes place effectively in direct band gap semiconductors in which the minimum of the conductance band and maximum of the valence band have the same momentum value. A direct, band-to-band, dominantly optical transitions are then possible. It is good to note that the spontaneous emission of LEDs yields relatively low irradiances in comparison to lasers. Figure 1 illustrates the simplified band structure of multiple quantum well (MQW) LED and the schematic depiction of the recombination processes of the charge carriers. The ABC transition arrows refer to defect-related Shockley-Read-Hall (SRH) recombination (A), radiative recombination (B) and Auger recombination (C). The ABC components affect the internal quantum efficiency (IQE) of an LED according to

$$IQE = \frac{Bn^2}{An + Bn^2 + Cn^3}, \quad (1)$$

in which  $n$  stands for charge carrier density. As it can be seen, only the B component produces desirable illumination and increases the IQE. The A and C components reduce IQE of an LED and are responsible for the so called droop effect, *i.e.*, decreasing quantum efficiency with increasing current. [5] The quantum efficiencies are intimately connected and the EQE can be defined to be the IQE times photon extraction efficiency (photon output divided by photon generation).

A traditional LED material is the quadratic compound  $Al_xGa_{x-1}As_yP_{y-1}$ . Subscripts y- and x- denote the percentage/amount of the corresponding element in the alloy. The emission wavelength of  $Al_xGa_{x-1}As_yP_{y-1}$  can be altered from infrared (IR) to green by changing the composition of the alloy. However, in the case of blue and white LEDs, gallium nitride (GaN) based LED-structures are used, because of the suitability of its direct, reasonably large band gap. The band gap of GaN is 3.4 eV. It can be alloyed with InN and AlN. Their band gaps are 0.7 eV and 6.2 eV, respectively. The peak wavelength of the GaN LEDs can be altered by varying the composition in indium atoms in a quantum well, or multiple quantum wells, in between the p- and n-type GaN. In IR-regime the most used material compound in LEDs is InGaAsP because its band gap ( corresponding 0,85  $\mu\text{m}$  wavelength) is tunable by a wide margin. Edge-emitting IR-LEDs are widely adopted as a light-sources in telecommunications technology. [6]

Fabrication of LEDs and other semiconductor materials are mainly done by epitaxial



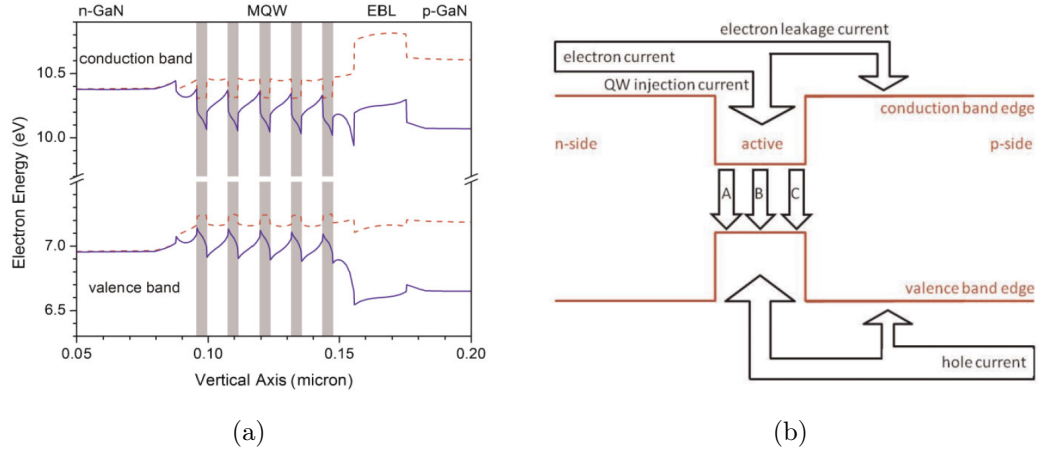


Figure 1: (a) Simulation-based illustration of the band structure of an InGaN/GaN MQW LED without (dashed line) and with (solid line) the effect of polarization fields. The electron blocking layer (EBL) is frequently used in LEDs to prevent electron leakage. (b) Simplified illustration of charge carrier paths in an LED structure. [5]

growth techniques known as metalorganic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE). MBE utilizes high purity source materials and ultra-high vacuum growth environment, which produce high quality films but also makes the operation and maintenance challenging due to demanding growth environment and quite slow growth rates. Thus, MOVPE is the most used method in research and commercial LED production as well as in III-N semiconductor growth in general. The precursor compounds in MOVPE consist of a metallic base atom, such as Ga, Al, In, *etc*, and organic bond groups which are usually hydrocarbons. With the right growth mode and process parameters, it can achieve the growth accuracy of almost a monolayer. In MOVPE, liquid phase precursors are brought in gas phase onto the surface of a heated substrate, where thermodynamical decomposition of precursors occurs and desired bonding reaction on the substrate surface is obtained. The flow of the precursors is facilitated by nitrogen or hydrogen carrier gases that also provide ambient atmosphere for reactions themselves. Typically, the group III and group V precursors enter the reaction chamber from separate gas lines and their amount is always accurately regulated with valves and mass flow controllers. [7]

In this Master's thesis used LED post-MOVPE process flow is described here as an example LED front-end process. After the desired semiconductor films have been grown by MOVPE, the current spreading layer (CSL) is evaporated on top of the wafer and annealed in order to obtain ohmic contacts. The semitransparent CSL is used to provide effective electric contact to p-GaN. CSL is typically a thin film of indium tin oxide (ITO) or a very thin (around 5 nm) layer of Ni/Au. A Ni/Au CSL was used in this work. The next step is to reveal the buried n-layer for the n-contacts. This is achieved with properly patterned photomask and photolithography step, followed by inductively coupled plasma reactive ion etching (ICP-RIE) process.

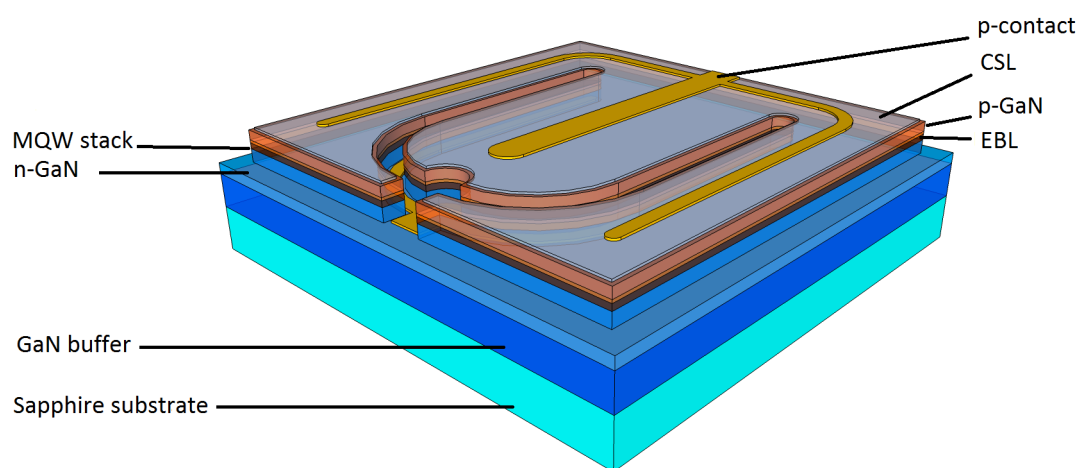


Figure 2: Schematic presentation of the GaN-LED geometry and the active layer design. The LEDs packaged in this thesis are based on the design shown here.

After that, the n-contact metallization (*e.g.*, Ti and Al) is sputtered or evaporated followed by the photoresist removal. Then, a second lithography-patterned metallization step (typically, Ni/Au) for the p-contact, is performed. Finally, when the resist is removed, one has obtained a front-end processed LED wafer. The processed LED structure on chip scale with all the functional layers is depicted in figure 2 and the described process flow shown in figure 3.

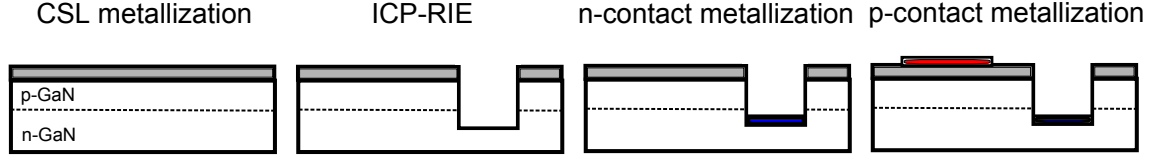


Figure 3: Main process steps in the front-end fabrication of a typical LED. The pattern transfer is performed with photolithography. The dotted line represents the optically active layer in between p- and n-type GaN.

After the LED is fabricated, the light it produces can be characterized by different kind of measurements and metrics. Especially, in the case of white light LEDs the correlated color temperature (CCT) and color rendering index (CRI) are used to define the quality of the light. In CCT, the Wien's law based color temperature of the illumination source is compared to the color temperature of an ideal Planckian radiator. The CRI is a quantitative measurand which compares light colors to an ideal natural light or reference light colors and it ranges from negative values to a maximum of 100. Incandescent lamps can achieve the value 100 and typical white light LEDs can provide a value above 80.

## 2.2 Wafer Singulation

This section covers the first part of the back-end processes: dicing. First, the main differences between typical dicing methods are being discussed. Then, a blade dicing which was used during the sample fabrication in this work is described in more detail.

### Wafer Separation Methods

Dicing is the first step of packaging where a processed wafer is separated into individual, functioning chips. There are a multitude of different kind of dicing methods which are being used in commercial and research purposes. Generally in semiconductor industry blade based dicing is still the most widely used separation method, although it is expected that laser based dicing methods will outdate the traditional dicers in the near future. Especially in LED and in many micro-electro-mechanical system (MEMS) component manufacturing the laser dicing has become the dominant dicing method due to better chip quality and lower running costs. Still, there are four significant separation methods which are currently being applied in semiconductor device manufacturing and these are depicted in figure 4. [8]

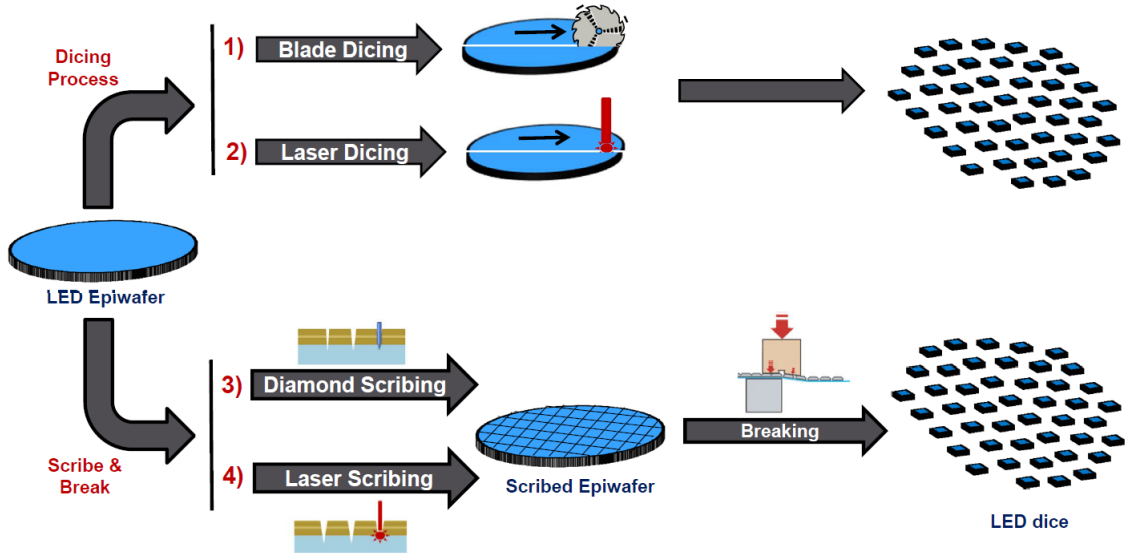


Figure 4: Four main LED chip singulation processes. [1]

One of the most traditional methods is to use an abrasive scraper, *e.g.*, diamond-based, to scrape a groove pattern on the processed wafer and crack the desired piece by applying mechanical stress. However, this is an inaccurate separation method due to the cracking property along a certain lattice orientations of the semiconductor wafers. That is why the diamond scraping is mainly used in research purposes when the wanted sample size and shape is not that significant. Some precision x-y-stage mounted and scribing force regulated mechanical scrapers have been implemented

but their chip yield and quality is not comparable to the other methods. [8]

Laser based separation methods can be divided into two categories: laser ablation dicing and to stealth dicing. In the laser ablation dicing, a pulsed laser with moderate fluence is used directly to evaporate the material from the dicing street. A different kind of chip geometries can be obtained by programming the laser to accurately scan the top of the wafer. The physical separation is achieved due to ablation in which the intense laser light excites the electrons and phonons of local lattice sites thus greatly increasing the lattice temperature. This leads to intense repulsive electrostatic forces between the ion cores of lattice which in turn causes them to break away from the lattice. These high-energetic ions and reactive particles may cause visual debris and are therefore needed to be vented or water-jetted off in order to avoid re-deposition on the processed wafer. Due to that, the laser ablation separated structures need a protective coating, such as spinned polymer film. For example on LED chip separation, the re-deposited aluminum and oxygen would diminish the light output and might even render the LED nonoperational. Also excessive laser fluency has been shown to generate poor dicing quality and thermally generated stresses to the chip. Ergo, laser ablation need to be operated in a certain moderate fluency range as presented in figure 5. Unfortunately this fluence is not enough for dicing wafers over 100  $\mu\text{m}$  thick. Therefore, the commercial laser ablation dicers are mainly designed for relatively thin wafers. Next generation ablation laser dicers promise to decrease the through-put-time of dicing process by implementing serial or parallel multi-beam laser dicers, thus providing multi-cut dicing. In total there are currently three commercial laser ablation technologies available, known as zero-overlap, multi-beam and water jet guided laser dicing technologies. [8–11]

In order to avoid the debris problem and the need for short-wavelength, high power lasers, more subtle laser dicing method called stealth dicing, also known as an internal modification dicing, has been developed and is already being applied in industrial semiconductor dicing processes. In stealth dicing, the separation is achieved by focusing a transmissible laser beam, usually IR, inside a wafer where the power is absorbed into the local lattice site, thus creating a defect area featuring voids, recrystallizations, dislocations and micro-cracking. These defects acts as a crack formation center. After the defect pattern is produced, the chip separation is achieved by applying an equal radial force on the mounting tape, as presented on process flow figure 6. The figure depicts also the usage of back grinding (BG) tape, test element groups (TEG) and die attach film (DAF), which are typically used in industrial dicing prosesses. [12]

Stealth dicing has clear advantages in comparison to laser ablation and blade dicing: it is a completely dry process, dominantly free of debris and post-process cleaning is not usually required. Thus, it is becoming a standard dicing method in semiconductor device industry and it is also being applied on LED chip separation. For example, Disco Inc. has developed stealth dicers for sapphire wafers [13]. According to Disco Inc., stealth dicing can achieve higher throughput and yield ratios than

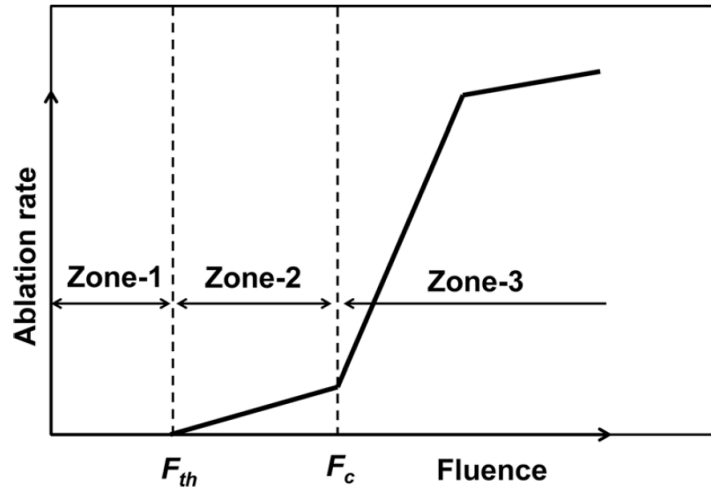


Figure 5: Plot of laser ablation rate vs. laser fluence. Feasible ablation fluence range is in zone-2. In zone-1 material evaporation does not occur and in zone-3 high fluence leads to chip damage. [8]

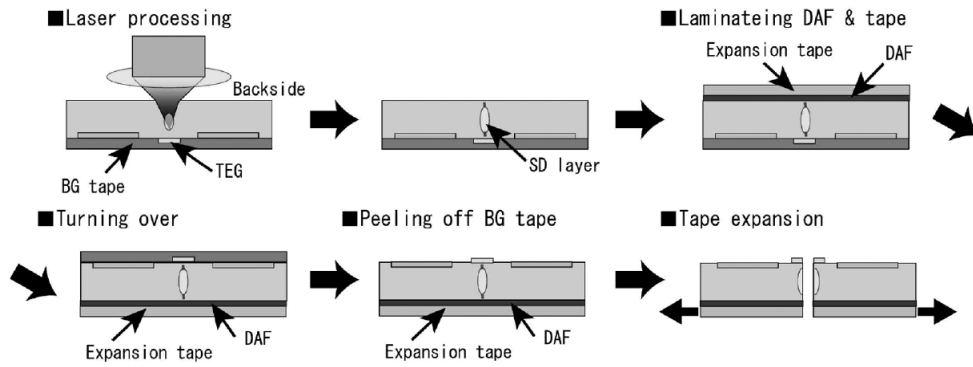


Figure 6: Stealth dicing chip singulation process. Laser induced internally modified layer is irradiated from the backside of the wafer and the final separation is achieved by radial tape expansion. [8]

more conventional methods. Still some disadvantages prevail. For instance, highly doped wafers introduce emphasized beam energy absorption before the focal depth is achieved, thus leading to insufficient damage volume formation and consecutive chip separation. Also, the laser beam focusing is problematic or impossible if the optical path includes opaque materials, such as metals. This also means that the dicing street widths needs to be potentially broad so that the materials would not affect the focusing of the laser beam and thus reduce the obtainable chip area on the wafer. [8]

Apart from these issues, it can be shown that other important dicing parameters can be further optimized in comparison to traditional blade based dicing. For example, the kerf width, *i.e.*, width of the cut, for mechanical sapphire dicing is around 150  $\mu\text{m}$ , while laser ablation can achieve 10  $\mu\text{m}$  kerfs, thus increasing the device-on-wafer yield. Also, the laser dicing is highly automated process and can provide higher productivity and lower running costs than mechanical singulation. [8–11]

Even though mechanical, laser ablation and stealth style dicing methods provide relatively fast and stable processes for wafer to chip separation, even more efficient and potent methods are being studied. For example, an optimized wafer plasma etching have been reported to provide promising results and some patents utilizing high-aspect-ratio deep reactive ion etching (DRIE) have already been published. [14] These methods have been proven to produce stress-free chips with extremely narrow kerf width. Also the shape of the chips is free to choose in this case. Also, wet etching have been applied to chip separation but the large consumed etching areas have been a major yield-reducing problem. The main advantage of industrial scale etch singulation still is the possibility to do large scale batch processing, because all the traditional methods are in-series processes whereas etching is in-parallel process. [8, 15]

In addition, so called filamentation technique has give a lot of promise as an immensely fast and convenient singulation method and is considered to be a candidate for the next generation dicing method. In this technique, a short wavelength, ultra-fast laser is used to fulfill a certain focusing and laser-power conditions which generate a plasma filament due to a very intense and localized electromagnetic-field. This plasma filament is formed inside the condensed matter consecutively dicing that area with superior edge roughness and scanspeed, achieving even 600 mm/s. The before mentioned focusing condition is achieved utilizing Kerr effect, in which a controlled electric field is used to alter the refractive index of the material, which allows the incoming laser pulse to focus properly. It ought to be noted that this Kerr effect induced plasma cutting is not the same phenomenon than the photon-electron-phonon induced laser ablation and does not have the same issues than in the traditional laser separation methods, such as unwanted reflections, die stress and edge roughness. In filamentation technique, laser fluency is above ablation threshold and with correct optics lead, therefore, to direct material removal. This technique is already applied on micro- and nanoscale drilling, such as through silicon

via (TSV) formation. However, its commercial applications on wafer dicing are not yet available. [15,16]

### Blade Dicing Process

Dating back to the beginning of microelectronics, the mechanical diamond blade dicing has been the workhorse of the semiconductor chip singulation. While more advanced singulation methods do exist nowadays, old-fashioned, blade-based dicing still is the predominant technique to achieve chip separation. This is so due to the flexibility and low capital costs of this mature technology. Still, the ever-increasing yield and performance requirements of semiconductor manufacturing processes are rendering mechanical dicing outdated. Especially in the industrial scale of LED manufacturing, the blade dicing have become obsolete. This can be accounted for the necessity to use processed wafers which are thinned and polished to be extremely thin, even 30  $\mu\text{m}$ , and therefore mechanically very fragile.

In mechanical blade dicing, there are many parameters that dictate the end quality of the process and need to be considered carefully. These parameters can be categorized as wafer, blade, process, wafer mounting and saw machine parameters. Poorly chosen parameters will result in premature breakage of the blades together with reduced yield and quality of the chips. The reduced quality can be characterized with many ways. One of the most notably of these is chipping, which means off-cracked pieces alongside the edges of the dicing street. Chipping can occur on top and bottom side of the wafer. If the chipping is severe enough, it can ruin the device layer of the chip in question. Large enough chipping will lead to the rejection of the chip in question. Chipping, kerf and street widths, *i.e.*, device-to-device distance, are depicted in figure 7.

Other dicing quality parameters include precision of kerf geometry, chips side wall damage (such as microcracks and dislocations), die surface contamination, electrostatic discharge formation, delamination and chip strength and dispersion. Especially on robust environment MEMS chip, the chip strength is important factor to maintain as high as possible. Blade dicing is known to induce mechanical stress and vibrations into the diced chips resulting in decreased chip strength. In order to reduce the effect of these failure mechanisms to minimum, one ought to be aware of the dicing quality parameters and, thus, those are considered here in more detailed fashion. Moreover, these parameter categories with their detailed subdivisions are presented in figure 8.

Depending on the material of the wafer, the parameters in the dicing recipe have to be optimized in order to avoid wafer or device damage. Notable material parameters which have to be taken into account for optimal result in dicing are brittleness, Young's modulus, crystal or non-crystal structure, *etc.*. For example softer silicon can be diced with much higher blade rotation speeds and feed rate speeds than the hard sapphire. Also, the thickness of the wafer and the materials on the dic-





Figure 7: Left: illustration of kerf and street. Right: illustration of dicing induced chipping.

ing streets affect the dicing results and ought to be considered. However, in the case of III-N LEDs, the effect of the street material can be neglected due to the small thickness and the structural similarity of the sapphire and epitaxial GaN. As a side note one might add, that also a silicon wafer integrated LED manufacturing processes are being applied and developed. Addressing such a challenging material combinations as GaN-on-Si is one example of the versatile engineering challenges of the LED blade dicing.

There are numerous kinds of blades for different material types and process requirements. In the case of blade dicing of GaN LEDs grown on sapphire, a hubless type, diamond impregnated blades on nickel alloy or vitric matrix material are usually being used. The grain size of the grinding diamonds and their density determine the wear rate and the overall life time of the blade together with the hardness of the binder material. In addition, process parameters such as rotation speed and feed rate affect the wear rate of the blade. Naturally, also the width of the blade affects these parameters. Usual width of a sapphire dicing blade is 100-300  $\mu\text{m}$  and the diameter is 2 or 4 inches [17]. However, in silicon dicing even 15  $\mu\text{m}$  blade widths are used, but such thin blades are extremely susceptible for breaking. When taking the wafer material in consideration, it can still be stated that the thicker the wafer, the wider the blade. Ideally the kerf width would be the same as the width of the blade but due to chipping the kerf will typically be 10 to 50  $\mu\text{m}$  wider than the blade itself. [18, 19]

The process parameters are usually tunable on the dicing equipment itself. In addition to the blade and the adhesive tape, they determine the actual dicing recipe and can be chosen to suit the wafer material under dicing. In the case of sapphire wafers defining the number of cuts required to cut through the wafer is an important parameter. While dicing hard materials, such as sapphire, it is beneficial not to cut through the wafer with a single cut. Dicing the wafer using multiple shallow cuts increases the lifetime of the blade and improves the quality of the kerf. The problem with the multi-cut mode is that it reduces the through put time. This issue is, however, solved on many dicers by integrating a second serial spindle blade to the dicing equipment. Another crucial process parameter is the feed rate which is the speed at which the wafer is fed towards the blade. It is given in mm/s and ranges from fractions of mm/s to tens of mm/s. In the case of sapphire it should be chosen to be slower than with silicon. High feed rates speed up the processing and increase the through-put but at the same time increase the risk of damage. Same applies to rotational blade speed as well; higher the speed, higher the damage probability. Blade has a tendency to start to waggle on high rotations per minutes (RPM), despite the extensive blade mounting. Other parameters in this category include geometry depended parameters such as cutting depth, wafer thickness, index step (distance between parallel cuts) and the length of the cut. [8, 18]

In blade dicing, wafer mounting is quite straightforward but important process where the wafer is usually attached to a metal rim tensed adhesive polymer film, also known

as die attach film (DAF), top side facing upwards. The DAF is usually cured thermally or with ultraviolet (UV) light in order to obtain high adhesion. Then the tape-wafer combination is mounted on a vacuum chuck of dicing equipment. Tape-to-wafer adhesion is important factor because small chips easily break away from the DAF either due to mechanical vibration induced by the blade, or due to the high pressure water jet, which rinses the loose debris away. In the case of large chip size (such as more than 1 mm x 1 mm), the DAF does not necessarily need to be UV or thermally curable because the larger attachment area promotes better chip-on-DAF adhesion. It should also be noted that the microscopic and macroscopic flatness of the tape need to be high in order to obtain a good dicing quality. Also its thermomechanical features need to be compatible with the intense conditions under the cutting blade. In addition, other mounting schemes do exist. The holding of the wafer can be done by vacuum, magnets, electromagnets or clamping. In a similar way, the mounting medium can be tape, cement or wax. The best holder system is always process and material dependent. [17]

Dicing equipment parameters are determined by the design and added features of the given dicer. This category includes for example spindle, stage, blade and flange balancing and mounting, alignment optics, cooling system and online process monitoring solutions. These factors can be summed up to mechanical design, cooling system design and the usability of the system. [8]

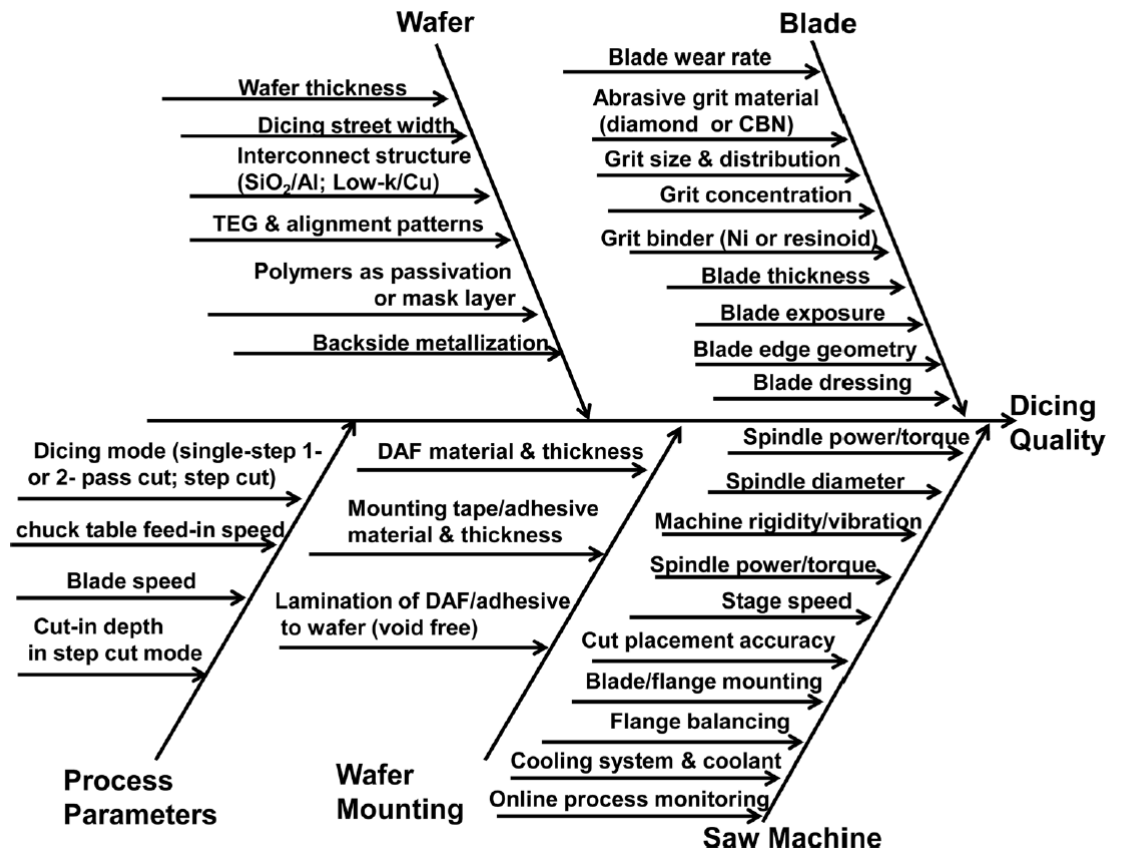


Figure 8: Fishbone diagram of the blade dicing quality. DAF refers to die attach film, TEG to test element group, CBN to cubic boron nitride. [8]

## 2.3 Chip Attachment

Chip attachment is the process of mechanically fixing the chip to the package. There are myriads of different kind of chip attachment methods in microelectronics such as solder die bonding, eutectic die bonding, glass die bonding and, the most common, polymer die bonding. In the LED attachment, the effective heat dissipation from the chip to the package is one of the most important properties of the die attach material, especially on the case of high-power LEDs (HPLEDs). The secondary requirement for the LED chip attachment material is its shear stress endurance. Shear stress is the mechanical force needed to detach the bonded chip and is an important bond quality test parameter in industry. In addition, some packaging assembly designs are based on back-side electric contacts and because of that require electrically conductive attachment materials. [20]

In LED-chip attachment, usually a traditional soldering, Au/Sn-eutectic or polymer die bonding are being used. These methods have their advantages and disadvantages. Soldering chip bonding provides the best mechanical stability in the terms of the measured shear tests and good electrical conductivity. On the other hand, Au/Sn eutectic bonding offers the highest thermal conductivity and heat transfers coefficient from these three. Despite these performance advantages, the polymer chip bonding provides a good compromise between mechanical adhesion, thermal conductivity and electrical conductivity due to its tunable material features and, above all else, simple process flow and low costs. [18, 20]

The procedure of polymer die bonding is straightforward and presented in figure 9. First, typically a two-component polymer consisting of epoxyhartz and hardening substance, is mixed in appropriate ratio. Second, the mixed polymer is applied to the package by dispensing, stamping or printing. Then the polymer is cured under appropriate treatment, *e.g.*, subjecting it to elevated temperatures. Noteworthy, many adhesive polymers also harden at room temperature given enough time. The advantage of using polymers is their low cost and their adjustable properties. By adding fillers like Au, Ag, Cu or Ni to the polymer, it can be rendered electrically conductive or thermally conductive. By altering the geometry and size of filler particles, an anisotropy of these properties can be obtained. If a truly effective electrical conductivity is desired, then usually a lead-based solder is dispensed and melted on mounting template and then the chip is pressed into that while the solder is still in liquid phase. In LED-chip attachment, one should always consider the amount of consecutive thermal stress load of the process, because it can be potentially harmful to the contact metallizations of the LEDs.

It is worthwhile mentioning that in industrial LED-chip attachment, primarily two different methods are being used. In low-power LED-chip attachment, previously described surface mount polymer die bonding is routinely used. However, in the case of high-brightness LEDs (HBLEDs), the necessity of efficient heat conduction and high light output require different kind of packaging design and process flow.

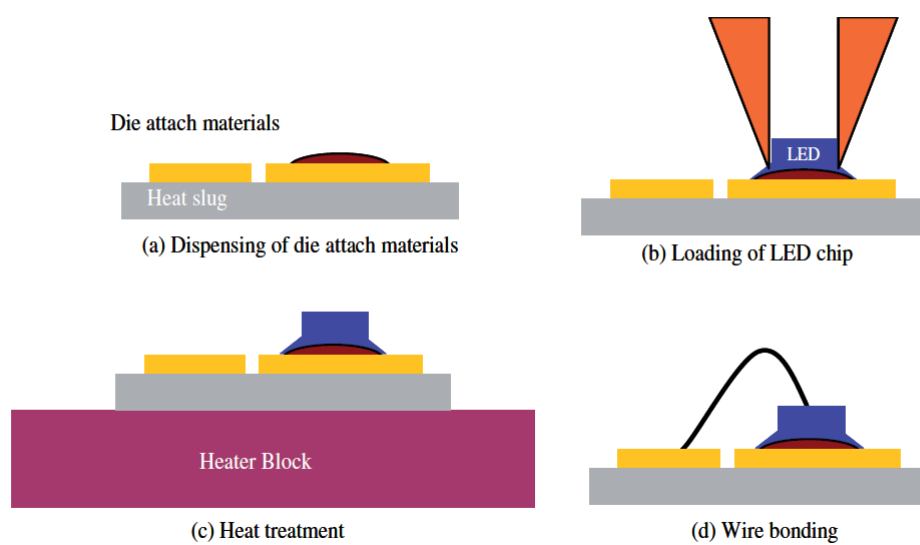


Figure 9: Schematic illustration of the die bonding process for die attach polymers or solder pastes. Attachment substrate works here also as a heat slug. [20]

Thus, the flip-chip mounting is widely used, where thinned LED chips have their front-side anode and cathode electrodes mechanically and electrically attached on the template substrate via solder bumps and proper metallizations. Galvanic and thermal connection from the chip electrodes to the mounting substrate can thus be obtained by heating the component to the melting point of the solder in question. In this approach, fragile bond wires are not needed, thinned substrate allows more efficient light emission and packaging process can be done partially on wafer level, hence potentially reducing unit costs. Downside is that the process is more complicated and include, *e.g.*, patterning and multistage metal depositions also on the LED-chip mounting substrate.

## 2.4 Wire-bonding

Wire-bonding is widely used method to establish electrical path from the contact pads of the chip to the leads of the package. In this section, an overview to wire-bonding devices, processes and quality features are given.

### General Overview

In microelectronics, there are mainly two methods to provide electric interconnections between the chip and the package: flip-chip bonding and wire bonding. In IC industry, wire bonding is still the most widely used method but in MEMS packaging the flip-chip assembly is dominating due to its multi-purpose nature, reliability and low costs in mass production. The most preferable method depends on the design and purpose of the MEMS device. Still, both of these methods can provide fast processing times, accuracy and reliability with advanced robotized automation, machine vision systems and intelligent algorithms. Also in LED manufacturing, both methods are being used and the technique of choice is determined mainly by the power requirements of the LEDs. Usually in research institutions and low-power LED manufacturing, manual wire bonders are still being used due to their simplicity, versatility and low costs, even though flip-chip bonding devices are becoming more and more common. [21]

In this thesis work, main focus is directed to wire-bonding process due to its convenience, availability and still high significance in the field of microelectronics. In addition, wire bonding provides highly conductive and stable electrical junctions, cost effectiveness, low mechanical and thermal loading for the chip, high speed, small chip area and compatibility to the micro manufacturing processes. It should be noted that also flip-chip bonding allows many of these advantages, together with more potent heat dissipation, combined chip attachment process and, in some packaging processes, even wafer-level packaging.

The wire bonding process can be described in general level even though many different kind of technical solutions are being applied in commercial wire bonders. As an example of the wire-bonding process, a simplified wedge-wedge-bonding is illustrated in figure 10. In wire bonder, the wire metal, which can be Au, Cu or Al, is fed through a carefully designed perforated needle tip so that the wire is out in a slight incline angle with respect to the tip. The wire feeding can be done by mechanical clamps that gently pull the wire from the wire coil. The needle can be then brought to a work height by a pre-programmed precision height control system. Then, the first bond can be done by pressing the wire with the tip with a certain force to the bond-terminal surface, while applying ultrasonic (US) energy to the wire and the joint. After a short US time, usually a few milliseconds, the clamps will open and the tip is lifted to a work height and if the joint was successful the needle can be moved above the destination bond contact and the solid wire will follow. Then the tip with wire can, again, be pressed to the surface end-contact under US energy, to achieve the second contact. Lastly, the wire is broken off by clamping it and moving



the needle. In this way, an arc-shaped, contact-to-contact wire bond is achieved.

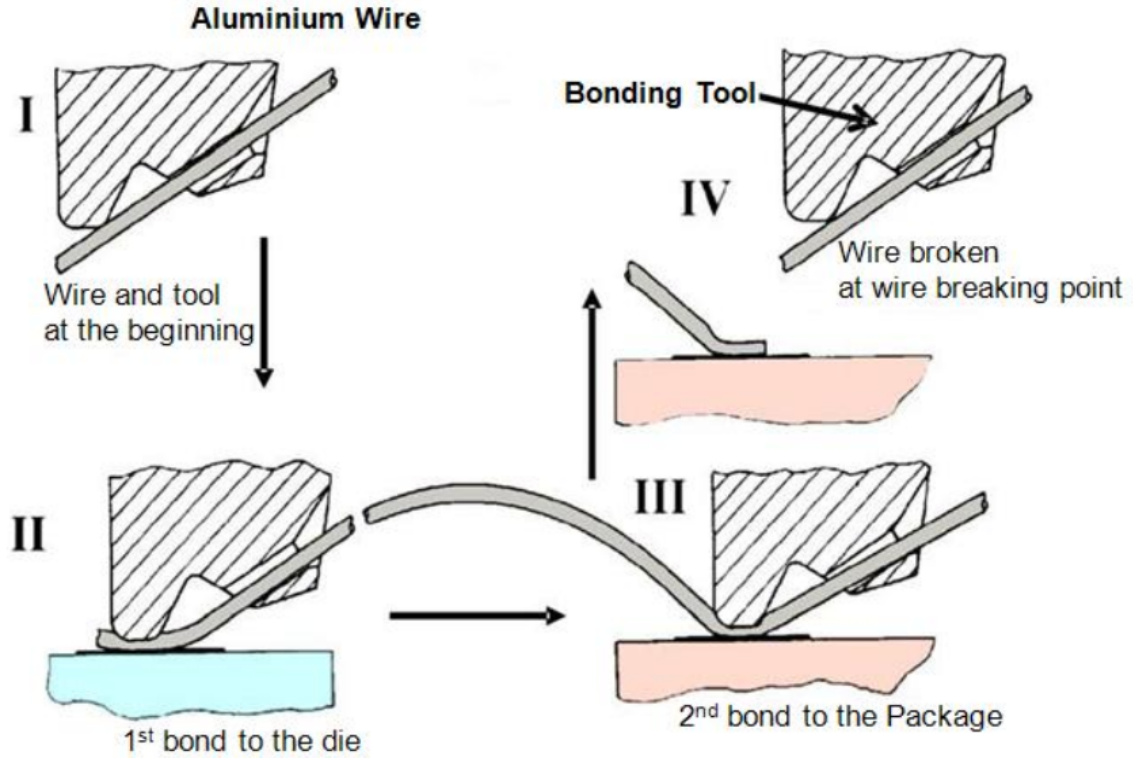


Figure 10: Schematic representation of the wedge-wedge wire-bonding process. [22]

### Wire-Bonding Techniques and Materials

Mainly two wire bonding techniques are being widely used: ball-wedge (b-w) bonding and wedge-wedge (w-w) bonding. Ball and wedge refer to the geometrical shape of the joining metal wire. The b-w bonding is slightly more complicated process than w-w bonding, because the initial spherical metal shape requires electronic-flame-off (EFO), an arc discharge induced melting process. The major advantage of the sphere-shape initial bond is that the moving direction of the wire is free to choose. Thus b-w bonders are especially used in automated, commercial back-end microelectronics manufacturing processes. In w-w bond the first bond determines the only possible direction of the wire feeding and means that the wire bonded structures should be aligned between adjacent bonds and not freely. However, the advantage of this bond process is that it is cold bonding, *i.e.*, no joint heating is required, and wedge-type endings do not require as much chip area as the ball-type.

Ball-wedge wire bonding is a thermosonic process, which means that during the first bond, not only the pressure and the US energy are applied but heating too. This is mandatory for gold wires due to the softness of gold in comparison to other metals

and a relatively low US-energy-respond of gold. Even high US energies would not suffice to form a proper metallurgical weld. The wire material selection for b-w bonders is more limited than for w-w bonder because the required heating forms unwanted oxides with common wire metals such as copper and aluminum. Due to that b-w bonders use usually gold wires, even though some copper wire compatible b-w bond processes under inert gas flows have been studied and used. [23]

In contrast to b-w bonding, the w-w bonding is purely ultrasonic and uses therefore usually aluminum and copper wires. The critical parameters are the contact force, surface friction and US energy and time. The US energy is introduced to the joint by a sonotrode, which is a piezoelectric transducer which transforms injected alternating current to a corresponding mechanical vibration frequency. The oscillation amplitude of the sonotrode is parallel to the substrate surface and perpendicular to the bond needle. The usual oscillation frequencies are tunable between 15-100 kHz and the coincident vibration amplitudes range between 12 and 150  $\mu\text{m}$ . The appropriate US-energy value depends on the hardness of the materials in question and the thickness of the wire, together with the type of the bonder. The applied US energy not only plastically deforms the wire metal and surface contact together but also physically cleans the pad surface from debris and thin oxide films by scrapping the joint surface. In addition to contact deformation, also inter-diffusion of the bond pad metal and the wire metal occurs further strengthening the cold weld. [18]

As stated earlier, the process parameters need to be carefully tuned in order to achieve high mechanical stability and to minimize the contact resistances. By choosing compatible wire and contact pad materials, one guarantees that an ideal mechanical strength and ohmic contact is obtained. Usual contact pad materials are metals such as aluminum, gold, silver or copper. This is especially true for the used standard chip packages, like transistor-outline (TO) headers or many ceramic packages. However, the chip contacts may contain many kinds of materials, ranging from semiconductors to metal alloys and might therefore form slightly non-ohmic contacts. In LEDs, the usual contact metals are gold based alloys (or ITO, as mentioned earlier) which form good ohmic contacts to the wires. This advantage is however easily partially lost because p-GaN and contact metal form a non-ohmic Schottky barrier yielding relatively high contact resistance. Alloying an ohmic contact to p-GaN have proven to be difficult but possible and that is why ITO based contacts are being used in commercial LEDs. The most important material parameters to match between the contact pad materials and the wire are hardness, adhesion, thermal and electrical conductivity and diffusivity.

In addition to the contact and wire materials, the diameter of the used wire should be considered, because wires with a small diameter will burn under high currents. Thick wires for their turn, will use unnecessary large area from the chip although they will exhibit lower overall resistances. Due to the drive current-to-wire diameter matching requirement, bond wires are being fabricated from 15 micrometers to several hundreds micrometers. The corresponding resistances for 1 cm long bond

wires are approximately 0.375 ohms to 0.002 ohms.

### Bond Quality and Failure Mechanism

There are many possible ways to ruin the wire bonding process and the most common failure possibilities are listed in table 1. The most common causes for failed bonding process are poor bond parameter set-up, contaminated bonding areas and sometimes unstable chip-package holder, *e.g.*, incline bonding stage. The unprotected wire bonded device should always be handled carefully. Even if the wire bond is considered mechanically stable in fabrication point of view, it cannot tolerate any mishandling.

Table 1: Wire bonding failure mechanisms. [24]

Wedge/ball bond detachment	Detachment of the bond from the chip contact or the package terminal, which takes place usually during the lifting of the bond needle from the pad. Common causes are contamination of the bond pad, mechanical instability of the leadframe or the package holder during bonding, non-ideal bonding parameters and bond pad corrosion.
Wedge/ball bond heel break	Wirebond is cut from the wedge or ball joint to the wire. Probable causes are improper bonding parameters, incorrect wire looping and peeling off due to mechanical force impact.
Midspan wire break	Breakage along the spanned wire, which can be caused by too tight wire looping or mechanical or corrosive damage in the wire.
Electrical shortcuts	Usually wire-to-wire or bond-to-bond short cuts are caused by incorrect bond placement or bond parameter settings.
Chip cratering	Damage to the chip under the metallic pad, which is usually induced by usage of too large force for pressing the needle or thermal treatment in b-w bonding. Can cause voids, microcracking and dislocations underneath the bond pad and thus higher contact resistance.

## 2.5 Transparent Encapsulation

The core purpose of encapsulation in IC and MEMS packaging from the environment is to provide protection to the chip and the wire bonds. Requirements depend on the purpose and functionality of the chip. In the case of LEDs, encapsulant has to be transparent, provide desired spatial radiation pattern, enhance radiation extraction and increase long term reliability. The main causes for LED malfunctions are moisture and dust that can diffuse through encapsulant material which create corrosion and electro-oxidation on the LED chip. In addition, intense light, vibration, shock, chemical contaminants and other hostile environments can cause operation failures. A proper optical encapsulant prevents all off these damage mechanisms as well as possible, thus providing long life time and reliability.

### Encapsulation Materials

Due to the importance of transparent encapsulation in packaging optical devices, different kind of encapsulation materials have been developed with optimized properties for different purposes. For LED encapsulation mainly two materials are being used: epoxy and silicone. In general, epoxies provide better adhesion, moisture protection and hardness in comparison to silicones, which in turn are softer and have higher resistance to photo-thermal degradation. This photo-thermal sensitivity can be seen as a discoloration in relatively high temperatures. That is why silicones are preferred on UV LEDs and HBLEDs, while epoxies are more common on low to mid-brightness LEDs. Since the LEDs used in this study are not HBLEDs, epoxy was chosen as the capsulation material. The wide popularity of silicones and epoxies stems from the mechanical, electrical, optical and thermal properties which have been extensively studied and can be altered within certain ranges. Both of these materials and their molding processes are also phosphorization compatible, which is vital for white light LEDs. [25]

In addition to these two encapsulant materials, also a separate optical lens materials are typically used in HBLEDs, in order to further enhance the light extraction. Especially refractive index matching between the chip material and the encapsulant should be considered. GaN, which is used in white and blue LEDs, has a large refractive index ( $n=2.4$ ) compared to typical epoxy. Problem therefore arises in the semiconductor epoxy interface, where total internal reflection narrows down the escape cone of the emitted light. The light which is reflected back from the mentioned interface is lost. Glass is traditionally considered to be the best optical material but it is more expensive than other options. Therefore, silicone lenses are being used due to their high transmission and favorable dispersion factor. Also thermoplastics, such as acrylics (PMMA), polycarbonate (PC), polystyrene (PS) and polyamide 12 (PA12) are being commonly applied as LED lens materials. In near future LED optics are predicted to shift to so called diffractive optical elements (DOE), which are surface microstructures used to guide beam behavior. These would provide convenient small and flat micro-optics and could be fabricated by lithographic or other microprocessing methods. The ultimate goal is to produce monolithic micro-optics

on the LED at wafer level. [2]

Alike chip bonding epoxies, also encapsulation epoxies are usually thermally curable two component systems, which are hardened through cross-linking reaction polymerization. The first component contains epoxy resin, which is a reactive polymer class containing epoxide functional groups. On a chemical composition, epoxide is a cyclic ether, *i.e.*, oxygen atom with alkyl groups, with three ring atoms or groups. Most commonly used epoxy resins are diglycidyl ether of Bisphenol A (DGEBA) and cycloaliphatic epoxy resin (CER). The DGEBA system offers good thermal resistance and high strength but poor radiation resistance, while the aromatic CER provides good radiation resistance and high glass transition temperature ( $T_g$ ) but low moisture resistance. The second component is usually an organic acid anhydride and is functionally a hardener and catalyser. Hexahydrophthalic anhydride (HHPA) structure is an example of anhydrides group hardeners, which offer especially good color stability during thermal aging. Molecular structures of these common epoxy materials are illustrated in figure 11.

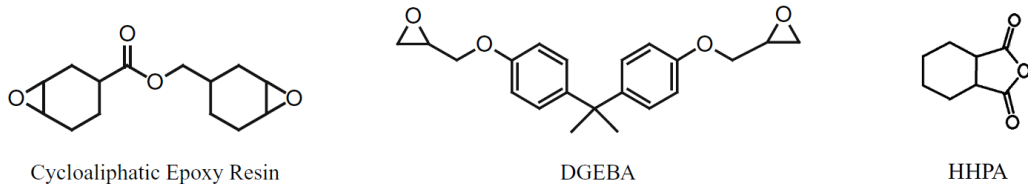


Figure 11: Molecular structures of the two most common epoxy resins (CER and DGEBA) and a hardener (HHPA) used in transparent LED encapsulation. [2]

In addition, many additives can be used in both components to improve the properties of the epoxy encapsulant. These include for example anti-UV agent, deformer, flexibilizer and antioxidants. By combining proper additives to prime components one can engineer important epoxy encapsulant parameters such as transparency, transparency retention upon thermal and radiation treatment, refractive index,  $T_g$ , coefficient of thermal expansion (CTE), viscosity, adhesion, flexural strength, modulus, toughness, moisture absorption and flame resistance [2]. [26]

Silicone polymer family forms a wide and tunable material class. They are basically partially glasses and partially organic linear polymers. The degree of hardness, brittleness, optical transmission and reflectance can be tailored in some degree by altering the amount of hydrocarbon groups, as can be seen in figure 12. It is this tunability, that makes the silicones so popular as lens materials, together with their excellent photo-thermal resiliency. The most used silicone is polydimethylsiloxane (PDMS) due to its relatively high refractive index of 1,40-1,60 and its favorable cure

chemistry. In HBLED packaging, at least two different kind of silicone compound chemistries are usually applied on encapsulation. For example, soft, gel-like silicones are preferred on optical lens molding, where as in chip encapsulation, more harder resins or elastomer type silicones are used. The curing of silicones is slightly more complicated than in the case of epoxies. The curing of silicones requires catalyzed addition, which usually is implemented by utilizing platinum complex cure system. [2, 25]

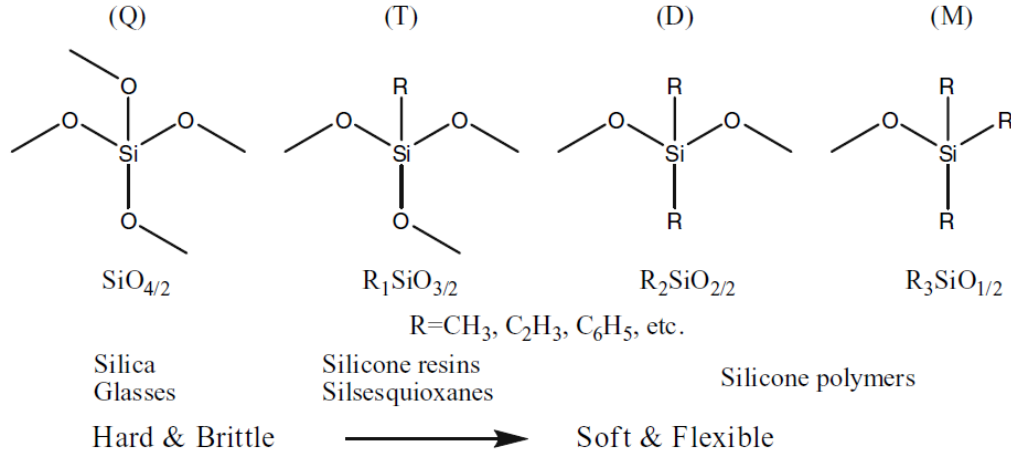


Figure 12: Examples of molecular structures in the silicone polymer family. Addition of hydrocarbon groups, denoted as a letter R, will render the material properties less glass-like. [2]

## Encapsulation Process

In transparent epoxy or silicone encapsulation of LEDs, the molding can be performed in different ways. One approach is to dispense the liquid lens material directly on top of the LED component yielding a dome shape encapsulation. Another way is to use a physical mold for the LED encapsulant. The casting method is commonly used in a simple LED lamp encapsulation while more sophisticated, solid epoxy based, encapsulation methods are being used in industry.

The dispensing of the dome material is a rather simple process and in industry it can be integrated to a wafer-level packaging (WLP) and especially on flip-chip assembly. In this process, the shape geometry and volume of the encapsulant can not be engineered as freely as in molding-based encapsulation. The surface tension of the liquid polymer in use greatly dictates the geometry of the dome. Also, the wettability of the liquid covered surface affects the dome form. There is, however, a possibility to engineer the contact angle of the lens dome. For example, R. Zhang *et al.* studied the effect of DRIE fabricated square trenches on the dispensed epoxy

droplet and found out that by altering the dimensions of these trenches, one can obtain some control on the contact angle [27]. It was also demonstrated that the ideal semi-sphere form (contact angle  $>80$  degree) can be achieved quite accurately with this method. In LEDs, a semi-sphere shape is usually desired due to the lambertian radiation pattern it produces. Similar results have also been reported by using shallow trenches cut by a blade dicer [28]. In HPLED encapsulation this kind of direct dome material dispensing as a part of flip-chip assembly is in some cases used because a complicated mold encapsulation process can be avoided. [29]

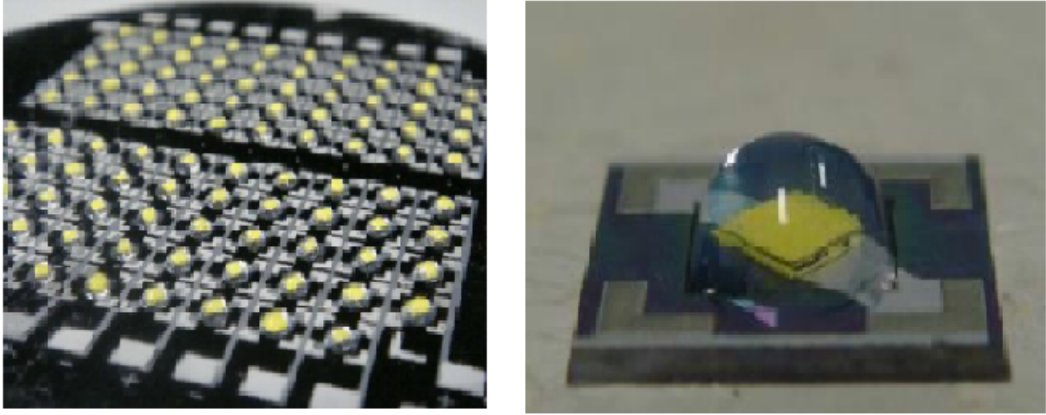


Figure 13: Left: photograph of wafer level encapsulated LED array. Right: photograph of a single LED component. [29]

Mold based encapsulation is more versatile process in terms of produced encapsulation shapes than the direct dispensing method. Encapsulation molds are especially used in the production of low-power LED components, IR-LEDs for telecommunication purposes and experimental encapsulation schemes like DOE. In this method semi-packaged LED is closed inside a casting module which is filled with liquid epoxy, or it is directly dipped to appropriately shaped and epoxy filled casting hole. Then the combination is cured. A typical mold casting process flow for simple LED lamps is depicted in figure 14. In commercial, high-volume manufacturing of LEDs, three molding processes known as transfer, compression and injecting molding are nowadays being used. These processes usually rely on solid epoxy pellets that are melted under appropriate temperature, vacuum level and mix-ratios. Then the liquid epoxy is led to the semi-packaged LED loaded mold cavities by compressive pressure. When the molds are filled with epoxy, the following curing treatment is done, yielding an encapsulated LED array. As an example of an industrial molding process, the transfer molding is presented in figure 15.

Transparent encapsulant molding can be considered straightforward but still failure-sensitive process. There are few issues which might cause a partial or a complete failure of LED encapsulation, such as incorrect-mix ratio-induced incomplete poly-

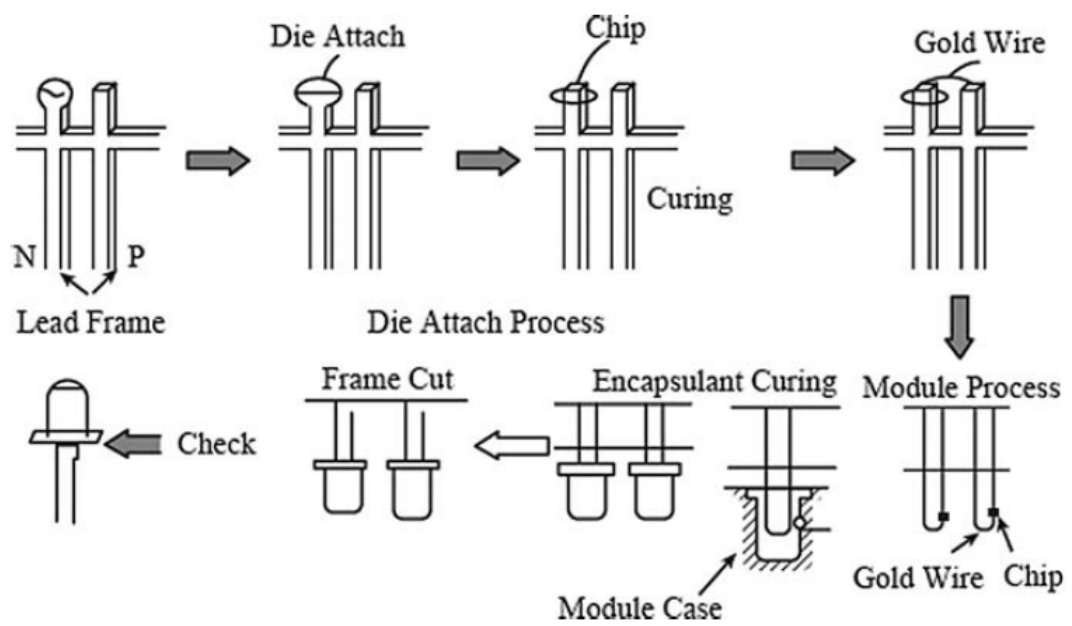


Figure 14: Basic, low-power LED encapsulation mold process. [2].



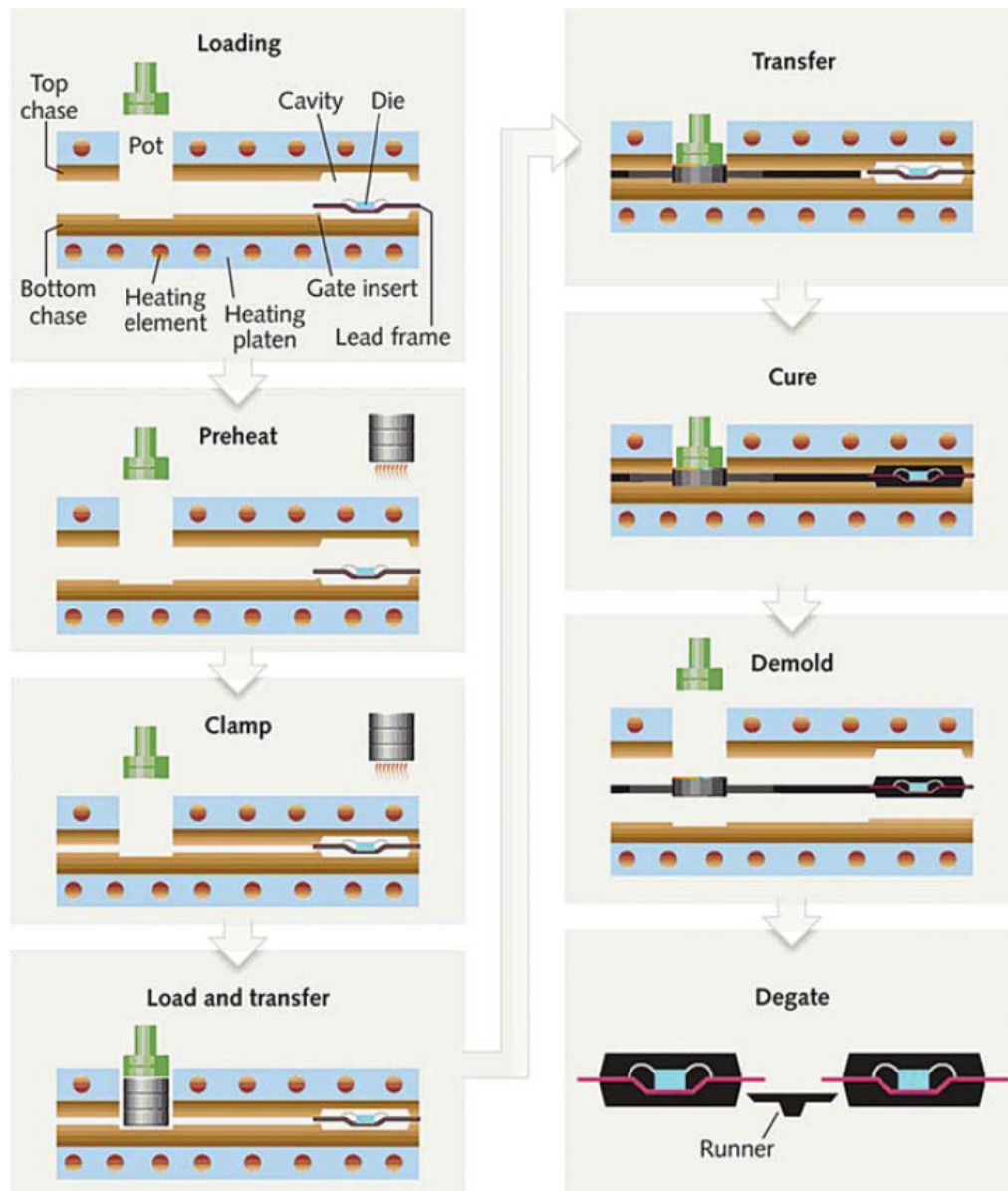


Figure 15: Schematic representation of transfer mold process which is commonly used for instance in high-volume optical device packaging. [2].

merization networking or void formation during the liquid encapsulation process. The first one of these is usually not a problem if the weight mix ratio is been carefully monitored and applied. In addition, contemporary epoxies are not very sensitive to a minor deviation from the exact mix ratio. Also, the alignment of the semi-packaged LED components into the mold can fail, yielding misaligned encapsulant dome.

As mentioned earlier, one notable practical problem with the mold encapsulation is the formation of voids in the encapsulant material. Voids can be defined to be gas bubbles with a radius of  $1\text{ }\mu\text{m}$  -  $1\text{ mm}$ . Voids smaller than  $1\text{ }\mu\text{m}$  can be considered optically insignificant and voids larger than  $1\text{ mm}$  a reason for device rejection. Many factors affect the formation of voids, such as curing temperature, surrounding pressure during hardening, degree of heterogeneity in the mixture, vessel-to-mold dispensing, ambient moisture and component insertion to liquid epoxy in the mold. In industrial polymer encapsulation schemes presence of voids are reduced practically to non-existence with a proper control of process variables, namely the ambient pressure. For instance, T. A. Ludström *et al.* in Ref. 30 observed that sufficiently low vacuum level ( $\sim 1\text{ kPa}$  absolute pressure) during resin molding processes produced void-free epoxy resins. Presence of voids in MEMS or IC polymer encapsulants has been reported to result in reduced life time of these devices. Moreover, voids together with ambient electric fields in polymers, such as in epoxy, have also been reported to accelerate the deterioration of the mechanical, optical and electrical properties of the polymer [31]. That is why practically void-free encapsulants are required in packaging of electrical devices.

## White Light LEDs

Due to their unique requirements, white LEDs have to be considered as a special case in packaging. Moreover, blue or UV emitting GaN LEDs are a necessity in white LED applications and are therefore briefly discussed here. Traditionally, white light LEDs can be fabricated in three different ways shown in figure 16. A direct approach is to use three different color LED chips, red, green and blue (RGB), to generate an overlapping tricromatic radiation distribution which is sensed as white light by the human eye. This solution offers high luminous efficacy, broad range of color temperatures and a very good color rendering index (CRI). Nevertheless, implementation of white light HBLEDs is problematic because at high drive currents the color spectrum has a tendency to shift towards red, yielding unbalanced CRI. In principle this can be bypassed by implementation of an individual current control of every chip but this would further complicate already intricate and expensive electrical readout and drive circuitry of the LEDs. Thus, white light LED lamps based on RGB-emitters are not yet practical at least on general lighting applications. However, there is also a highly experimental suggestion to epitaxially grow quantum wells with different peak wavelengths in one LED structure resulting in a white light LED. [2, 25]

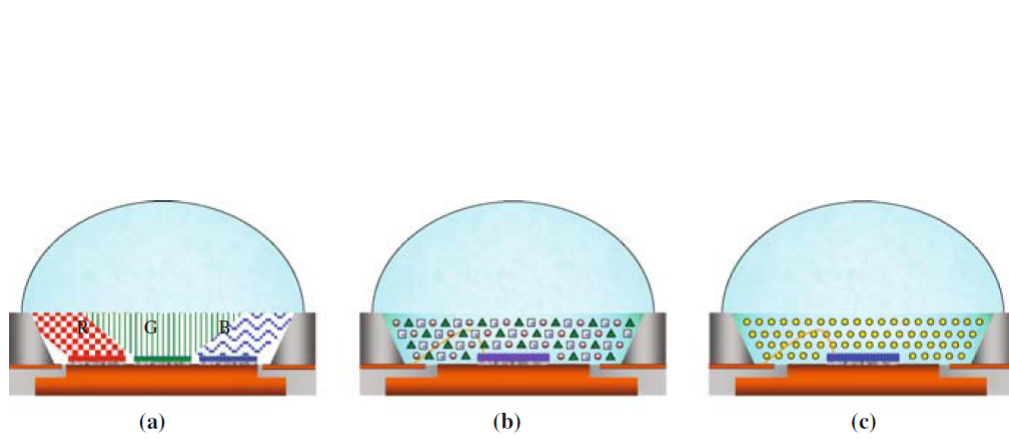
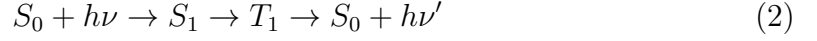


Figure 16: Three possible methods to produce white light emitting LED components: a) RGB color LED chips under single lens, b) an UV LED with RGB phosphor and c) a blue LED with yellow phosphor. [2].

The two other methods for white light LEDs are based on photoluminescence, more specifically phosphorescence, in encapsulant embedded phosphor materials. Phosphorescence differs from, also widely known, fluorescence phenomenon on its excitation dynamics which in phosphors is typically a so called triplet-singlet process and is presented as



where S denotes singlet and T triplet spin-states, while subscripts 0 and 1 describe occupation states, 0 being ground state and 1 excited state. The  $h\nu$  and  $h\nu'$  stand for energy of a short wavelength photon emitted from the LED and of longer wavelength down-converted photon, respectively. The relaxation times in this process are usually in the order of milliseconds but can also be hours for some phosphor compounds. There are a wide range of different phosphor materials corresponding to certain absorbance and radiated wavelengths and their excited state lifetimes. In the case of white LEDs, mainly blue light excited, yellow light emitting cerium-doped yttrium aluminum garnet ( $\text{Ce} : \text{Y}_3\text{Al}_5\text{O}_{12}$ , YAG:Ce) phosphor is used. It provides the highest possible blue-to-yellow down-conversion efficacy but its lack of red luminescence reduces achievable CRI. This results in blueish white light which is usually experienced as a cold hue, in contrast to actual color temperature which is high. That is why some white light LED applications mix RGB emitting phosphors in encapsulant, thus producing more "warmer" white LEDs on the detriment of EQE. In these types of RGB-phosphor LED components, an UV-regime LED chips are usually required in order to obtain energy down-conversion. However, the quantum efficiency of blue LEDs is far superior compared to UV LEDs. Additionally, the mature yellow phosphors used with blue LEDs have better down-conversion efficiency than the RGB-phosphors used with UV LEDs. [25]

There are mainly three ways of embedding phosphor into the LED package. The most direct method is to mix appropriate amount of phosphor particles into the encapsulation material and perform the encapsulation in normal fashion. However, the measured CCTs and white light uniformity are degraded because phosphor particles settle in uneven distribution during the curing process. This low CCT is still prevailing in many commercial LEDs. However, alternative methods to avoid these problems have been studied and implemented also in commercial LED manufacturing. One of these methods is conformal phosphor dispensing or deposition, in which the phosphor material is directly dispensed or deposited on top of the LED chip, prior to the encapsulation. The layer of phosphor is spread equally thickly on the chip, thus obtaining a conformal emitted color distribution. The accuracy of this phosphor coating is such, that the presence of wire bonds would harm it and that is why it can only be performed effectively on flip chip assembly. For instance, Luxeon HBLEDs use this patented method and have achieved better CCTs compared to their competitors. [2, 25]

In addition, a method called remote phosphor technique has been proposed to solve the above mentioned difficulties. In this method, the phosphor layer is not located in contact with the LED chip, so the down-conversion of light occurs away from the chip surface. This separated phosphor layer enables higher light extraction and reduced associated thermal loading due to the more advanced emitting layer and ambient encapsulation design possibilities. [2]

### 3 Developed Process for LED Packaging

This chapter describes the developed experimental process used to package LEDs fabricated in Micronova.

#### 3.1 Dicing

The LED wafers were singulated to chips with a dicing saw (MicroAce 3, Loadpoint Ltd.). The dicing parameters were optimized with 2-inch 430- $\mu\text{m}$ -thick sapphire wafers. The blade used in this dicing process was 150  $\mu\text{m}$  thick, resin bonded, hub-less type and had a diameter of 2 inch. Figure 17 shows a photograph of the used dicing equipment.



Figure 17: Blade dicing saw used in dicing the LED wafer without the blade or the wafer mount chuck.

Before the dicing process is started, it is important to attach the sample properly on a dicing tape and holder combination and strengthen the adhesion by curing it in an oven at 50 °C for 15 min. This is especially important if the intended chip size is smaller than 1 mm x 1 mm. The operation of the dicing equipment includes

various technical process steps from set-up to shutdown that are reviewed briefly in appendix A. The actual process parameters which were defined are listed in table 2. In that table, the mode 43 refers to device specific rectangular auto-mono dicing mode in which the through-wafer dicing is performed on two consecutive cuts.

Table 2: Determined dicing parameters for 430- $\mu\text{m}$ -thick, 2-inch sapphire wafers. The parameters like index step and number of cuts are omitted and should be defined regarding the operator's process requirements.

Dicing parameter	Value
Mode	43
Feed rate (mm/s)	0,3
Spindle speed (RPM)	12 000
Depth of cut (mm)	2,860
Component thickness (mm)	3
Dimension A and B (mm)	50
Blade thickness ( $\mu\text{m}$ )	150 or 250

### Protective Polymer

The damaging effect of the water jet and loose debris was studied with protected and un-protected LED wafers. The protection used in the dicing process was spin coated polymer film (resist AZ4562). The dicing of the un-protected wafer experienced some severe scratches on the metal films on top of the wafer, while the protected wafer was intact after removing the protective polymer. However, it was observed that removing of the polymer itself can cause damage, if the cleaning process is not performed with care.

To optimize the resist removal process, the singulated chips had to be separated from each other during the US acetone treatment. Therefore, a polyoxymethylene (POM) plastic dipping-tool featuring single chip pockets was designed and produced. This tool increased the yield and quality of the resist removal of the chips significantly. The resist removal process for post-diced LED chips was done with the following steps: 10 minutes in acetone with US energy, 5 minutes in isopropanol alcohol (IPA), 2 minutes in water and drying with the nitrogen blast gas gun. After that, microscope inspection of the chips was always performed, and only the chips showing high-quality surface were selected to the next stage. It should be noted that in some cases the chips required a longer acetone solving and US time than 10 minutes, in order to get rid of all the organic residues on the chips.

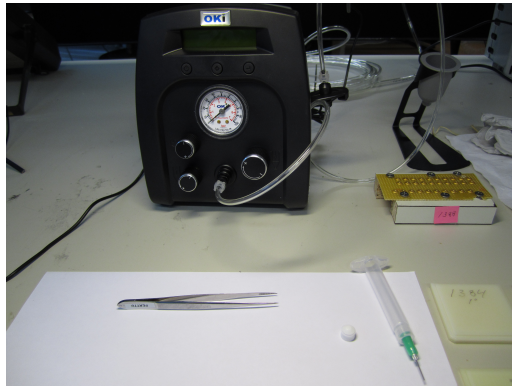
### 3.2 Polymer Chip Attachment

The processed and diced LED chips were attached to TO-46 headers. The TO-46 header was selected for its convenient size and suitability for our LEDs. The epoxy for die attachment was EPO-TEK H20E (Epoxy Technology Inc.). The H20E is a two component epoxy with silver particles mixed in. The epoxy was selected for its high adhesion as well as its thermal conductivity, which is as high as 2.5 W/mK. The epoxy is widely used for chip bonding in microelectronic and optoelectronic applications but is also used for thermal management applications. The technical data sheet and suggested applications of this epoxy can be found in appendix B. It should be noted that the epoxy components are skin irritating and thus wearing protective clothes while working with those is highly recommended.

The dispensing of mixed bond polymer was achieved with a pressure operated precision injection needle delivery system (depicted in figure 18(c)), thus obtaining high accuracy of the delivered amount and the positioning of the polymer. The dispensing device was Precision Dispensing System, DX-250. The other dispensing method experimented was a simple tooth-pick dispensing of mixed polymer which also is a viable method when header and chip sizes are relatively large, as in this case.

After the LED-chips are positioned to the epoxy on the header, the combination need to be cured in oven. The cross-linking of this epoxy follows roughly Arrhenius equation, which dictates exponential dependency of reaction time to temperature. In this process an annealing temperature at 120 °C and a consecutive time of 15 minutes were used. Higher temperatures than 120 °C begin to be detrimental to the used flame resistant 4 (FR-4) header platform and are thus not recommended. The developed attachment process is described in more details in appendix C and consecutively depicted in figure 18.





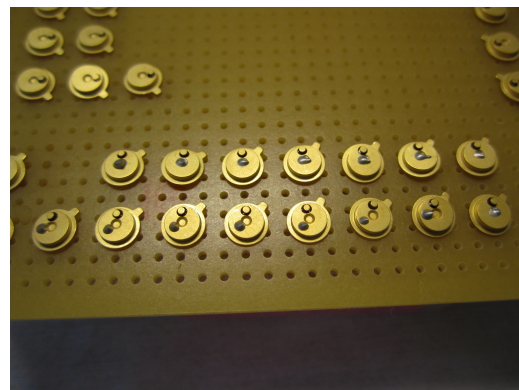
(a)



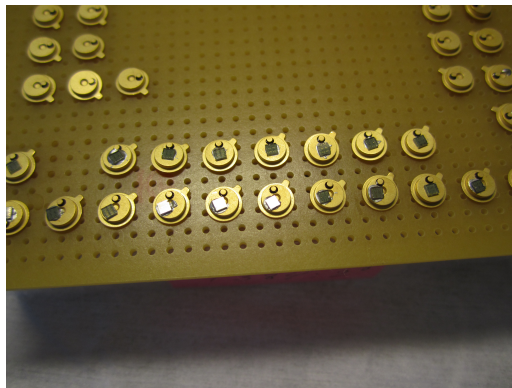
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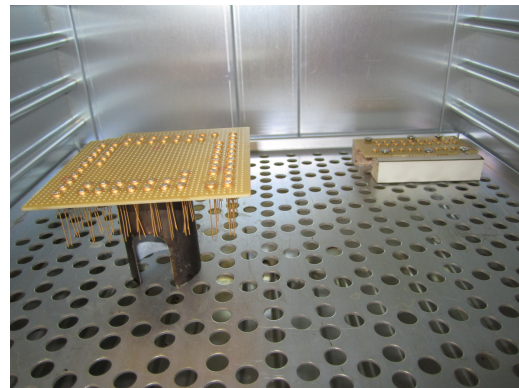
(c)



(d)



(e)



(f)

Figure 18: Depiction of polymer attachment process steps. (a) dispensing setup preparation. (b) mixing of the two-component conductive bond polymer. (c) loading of the injection needle with the bond polymer. (d) dispensing of the bond polymer to the headers through a pressurized injection needle. (e) LED-chip placement onto the bond polymer. (f) curing the combination on elevated temperature for a certain time.

### 3.3 Wire-bonding

The wire bonding process for the LED chips attached to TO-46 headers was developed for F&K Delvotec model 5330 wedge-wedge type wire bonder. Figure 19 shows the device in question. The bond process parameters were defined for stacked LED-package holder and the metal rim spacer depicted on the image. This spacer can be found on immediate vicinity of the wire bonder. The bonding process itself is observed through optical microscope which needs to be focused on the surface of the chip-header combination. The idea is that on the searchheight, the bond needle and the bonding plane are both in focus thus providing 3D vision.

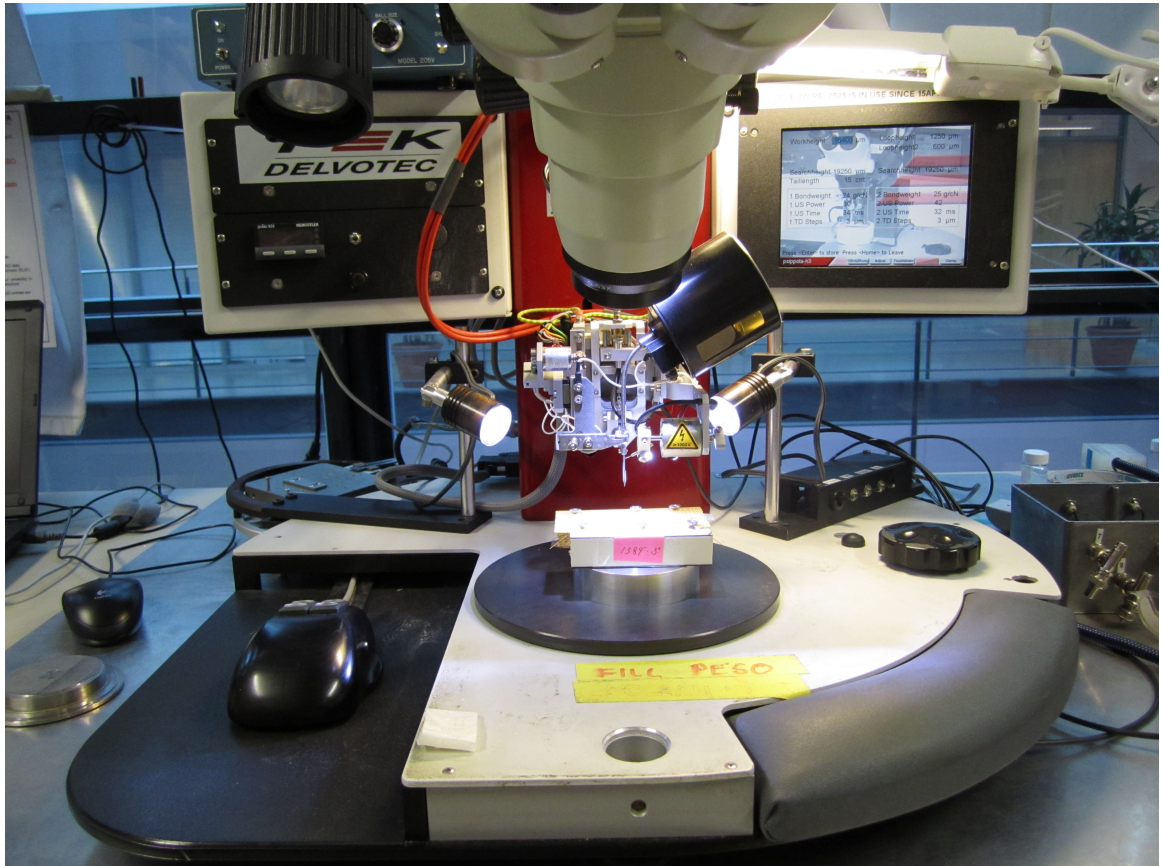


Figure 19: Photograph of the Micronova wirebonder with the sample holder under the bond needle.

Table 3 enumerates start and destination bond parameters and table 4 shows the height step parameters for the before-mentioned header holder and wire bonder combination. One should be aware that the described bond parameters might be needed to be defined again in the case of alterations to the device or materials, such as bond wire diameter changes or device maintenance. The developed wire bonding process is shown in figure 20 and a more detailed process step descriptions are provided in



appendix D.

One hampering practical issue in this specific wire-bond process was the relatively small area of the bonding pads of the LED chips (diameter being around  $50\text{ }\mu\text{m}$ ), which made it difficult to aim the needle. Thus, it would be wise to consider and alter the bond pad design so that the contact pads were large enough for bonding. Moreover, one common problem was that the wire feed tended to get stuck or that the wire was displaced from the hole of the tip. This problem is typical for this wire bonder device and it can be resolved with simply feeding the wire through the hole of the needle by lock-tweezers, or, in the case of stuck, solving the tip on IPA under US energy.

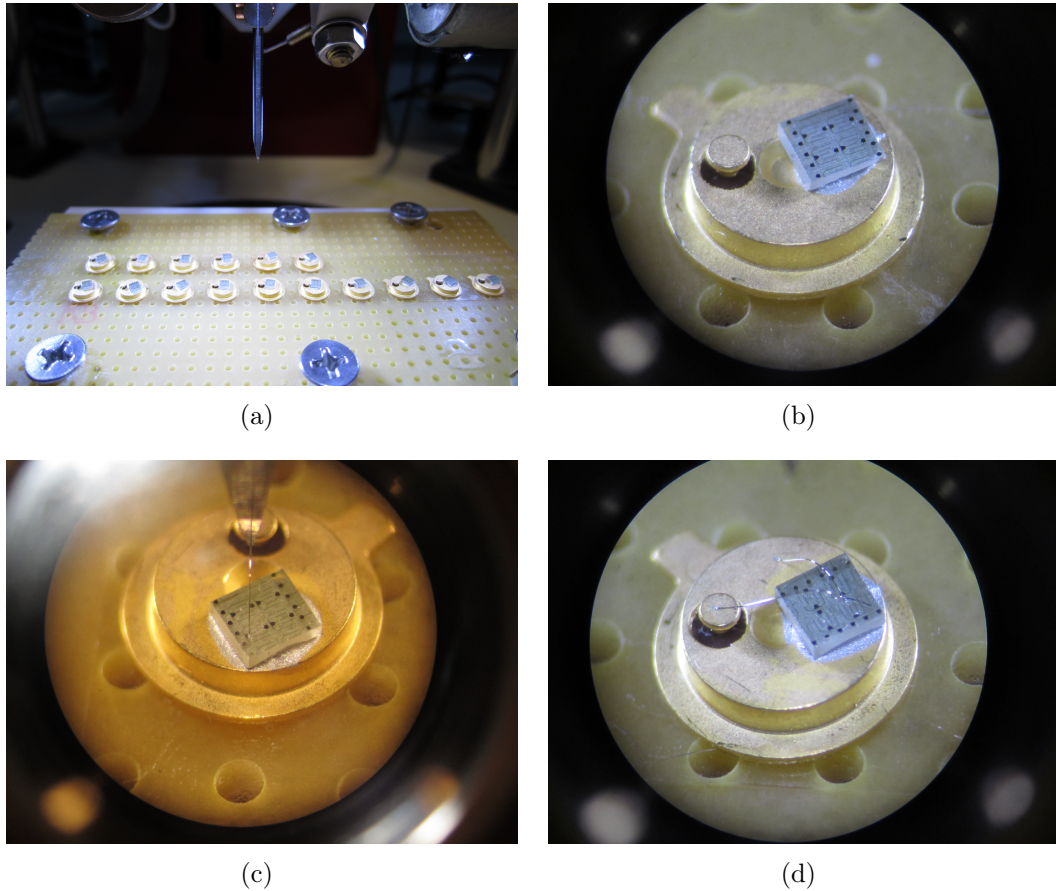


Figure 20: Photographs of manual wire bond process stages. (a) Bond needle on initial home position on top of LED packages. (b) Attached chip seen through properly focused microscope. (c) A successful pad-to-package bond and the needle on searchheight. (d) The wired LED chip after the second wire bonding process.

Table 3: Start and destination bond parameters for 25- $\mu\text{m}$ -diameter Al wire. TD step stands for touch down depth from the pad surface

Bonding parameters	Chip side	Header side
Bondweight (g/cN)	24	25
US Power (a.u.)	30	42
US Time (ms)	34	32
TD Step ( $\mu\text{m}$ )	3	3

Table 4: Height parameters for two-step bond process for LED chips on the specific holder in the wire bonder 5330 of Delvotec. The values are given in micrometers.

Process step	Value
Workheight	15400
Searchheight	18400
Loopheight	1250
Loopheight 2	600
Searchheight 2	19250

### 3.4 Epoxy Encapsulation

The developed epoxy encapsulation process for semi-packaged LEDs was based on silicone molding. The process for silicone mold casting using the fabricated molding stage device and the actual epoxy LED-encapsulation process are being described below.

#### Silicone Mold Casting

A room temperature vulcanizing two-component (RTV-2) silicone was used as a mold material due to its favorable mechanical properties, such as high tear strength, excellent mold-to-mold form factor and very low adhesion to resins. The chosen silicone was Elastosil M 4601 (from Wacker Chemie AG). The technical data sheet can be found in appendix E. The mold casting process using the in-house produced LED-encapsulation device is illustrated in figure 21. The depicted process is described in the same order in appendix F.

In order to obtain a high-quality, air-bubble-free silicone mold, it is paramount to subject the liquid silicone to a subsequent vacuum treatment. It was noticed that after the vacuum treatment the air bubbles tend to conglomerate on the surface of the silicone. After that it was easy to break them with a delicate mechanical contact. This same treatment applies also to the air bubble reduction on actual epoxy encapsulation. Due to the low adhesion to the mold casting device, the cast and the hardened mold can be easily replaced by twisting slightly the side of the silicone mold and simply lifting the mold away. Then a new mold can be fabricated.

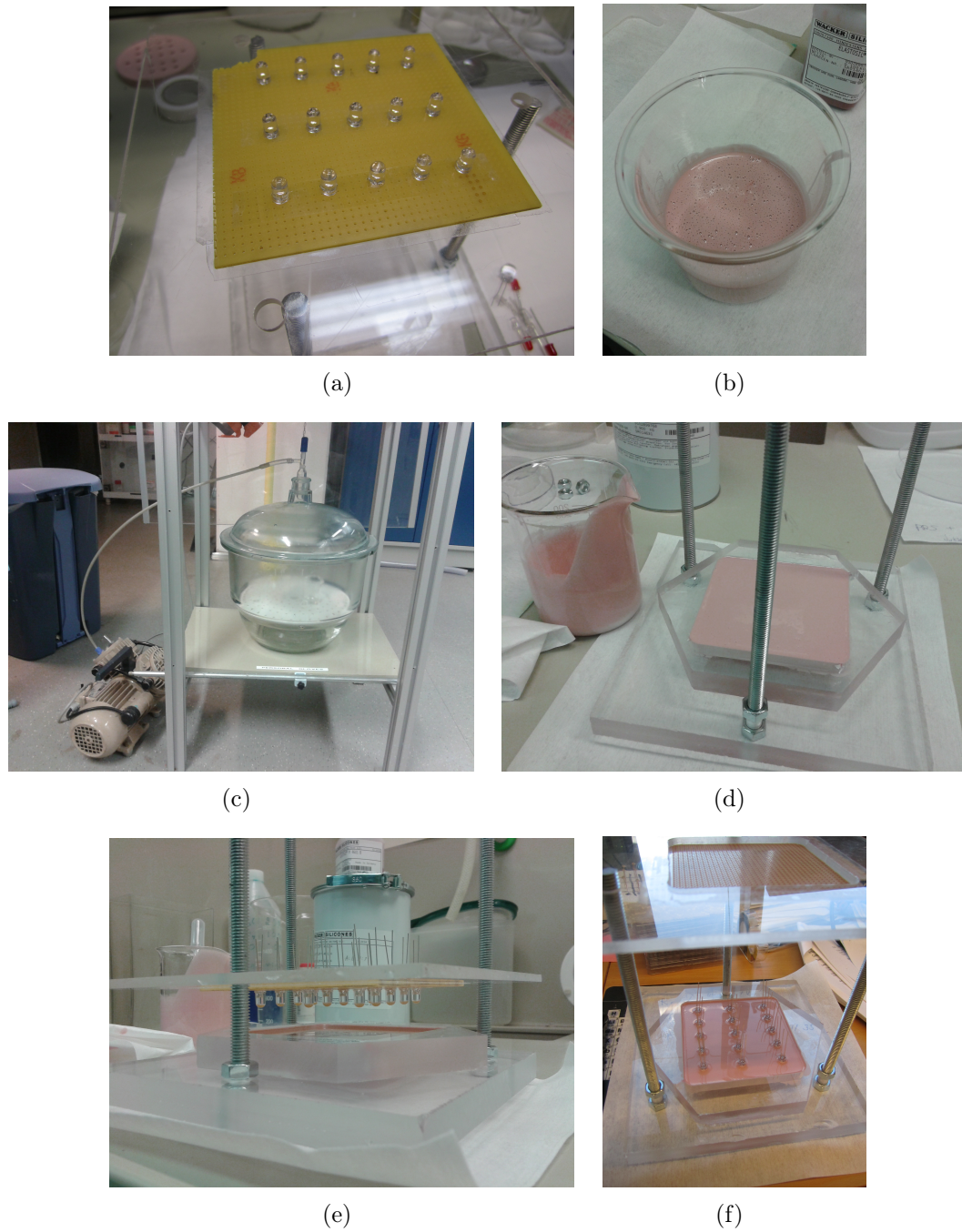


Figure 21: Presentation of the silicone LED-mold process flow. (a) The encapsulation device and molding component holder (FR-4) preparation. (b) Mixing of two-component silicone. (c) Air bubble removal in vacuum desiccator setup. (d) Dispensing of air bubble free silicone to molding cavity. (e) Bringing the copy-stage to a contact with the silicone through the screw rod, followed by 24 hour hardening time. (f) Lift-off of the copy-stage and a consecutive mold-component removal.



## LED-encapsulation

The LED-epoxy casting process is presented in figure 22. A two-component, optically transparent epoxy EPO-TEK 301-2FL (Epoxy Technology Inc.) was chosen due to its optical and mechanical properties that were designed and developed for optically transparent device packaging. The epoxy needs to harden either at 80 °C oven for 3 hours or at room temperature for 3 days. Only the latter method is advisable because the curing in the oven seemed to increase the void formation considerably. Appendix G presents the technical data sheet of the epoxy with handling instructions. The epoxy casting is performed on the silicone mold in the mold stage described previously.

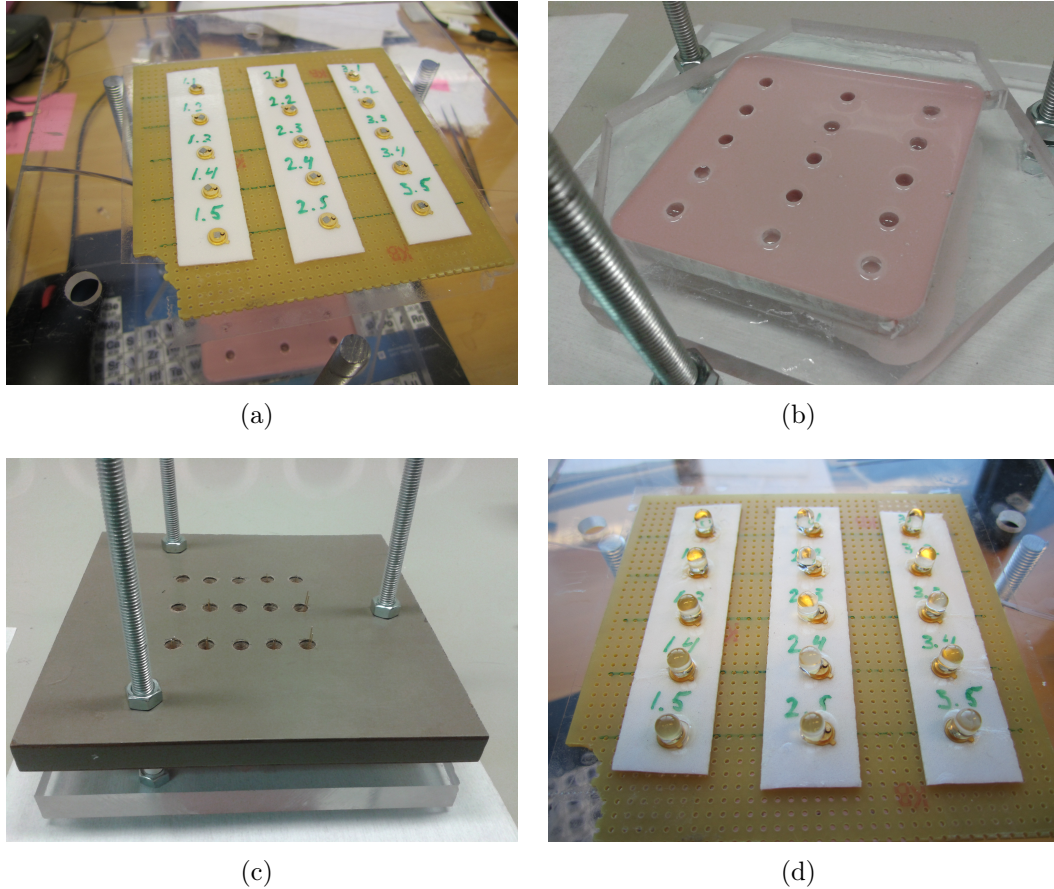


Figure 22: Process stages for the epoxy dome molding. (a) The preparation of the encapsulation device and partially packaged LED components. (b) Mixing, vacuum treating and dispensing of epoxy to the mold holes. (c) Mount stage stacking on top of the mold stage and room temperature three day curing. (d) Detachment of the mold stage by lifting and sample inspection.

The developed dome molding process for LED packaging can be roughly divided into four steps as depicted in figure 22. A more detailed molding process description is presented in appendix H.

## 4 Measurements

For this thesis, InGaN/GaN SQW LEDs were grown on sapphire wafers by MOVPE. These wafers were processed to LED chips (depicted in figure 2) according to the front-end process flow described briefly in section 2.1. All of the process development and following experiments were conducted on these in-house produced LEDs.

### 4.1 Characterization of LEDs

There are myriads different kind of characterization schemes covering optical, mechanical, thermal and electrical measurements that can be conducted to LEDs in different phases of manufacturing. Due to the nature of this thesis, the characterization of front-end LEDs and semiconductor nanostructures is omitted here and the measurement techniques like atomic force microscopy (AFM), x-ray diffraction (XRD), Fourier transform IR (FTIR) and many others are, thus, not described here. The viable measurements for back-end processed LEDs can be roughly divided into general testing of packaged LED components (mainly light emission related tests) and into process stage related tests. The latter ones are already shortly discussed in the background section and are only briefly reviewed here. However, the overall light output of packaged LED components is the most important performance metric and is thus also studied as a part of this process development.

Perhaps the most important measurement for LED components in general is the electroluminescence measurement. Typical properties under interest of an LED, which are characterized with EL measurement setup, are irradiance, radiant flux and the emission spectrum. From these, EQE and overall efficiency can be derived. The EL measurement setup will be presented in more detailed fashion in the following sections.

Luminescence can also be obtained with other methods than with a direct current injection in EL. For example, photoluminescence measurement is widely used as a basic characterization method for the LED structure. In the measurement laser beam is focused onto the sample. The energy of the photon from the laser has to be larger than the band gap of the examined semiconductor. The incident photons excite electrons from the valence band to the conduction band. The excited electron relaxes back to the valence band with the possibility to emit a photon corresponding to the band gap energy of the semiconductor. The advantage of the PL measurement is that it allows to characterize samples without processing metal contacts to the structure.

The same excitation can also be obtained with cathodoluminescence (CL) measurements. In CL, electrons from the source are injected with high electric field into the desired semiconductor structure, thus producing valence-to-conduction band excitation and consequent light generation due to recombination. CL is especially viable for mapping optical activity of low-dimensional semiconductor structures, such as



QWs and quantum dots. In addition to these spectroscopy measurements, other optical characterization methods do exist and are extensively used in commercial LED production and product development. These methods include spatial light emission pattern mapping, correlated color temperature (CCT) and color rendering index (CRI).

Current-voltage (I-V) measurement is one of the most important electrical characterization methods for a diode structure, hence also for LEDs. In this measurement, metallic probes are connected to the contact pads of the LED chip and voltage is swept from a certain negative value to a positive value while measuring the consecutive current values. From the obtained graph, one can easily see, for example, the diode nature of the pn-junction and the ohmic character of the metallic contacts. Main parameters determined from the I-V measurements are typically the forward threshold voltage together with the overall series resistance of the LED structure. Another standard measurement for LEDs is light output power as a function of injected current. This measurement is also important in characterization of thermal properties of the LED structures due to the induced Joule heating. The thermal properties can be further measured with, for example, a calorimeter, IR-imaging or a thermometer on the heat sink element.

In addition to illumination, thermal and electricity related measuring schemes, there are various process-stage-dependent measurements which concentrate on the overall quality of the given process step. For instance, LED chip dicing process measurements might include stress tests, edge roughness monitoring, post-dicing particle mapping and also various possible in-crystal or active layer damage test to find out induced defects like dislocations, voids and micro-cracks (can be tested with, *e.g.*, FTIR or XRD.)

Characterization of chip attachment quality can include mechanical, thermal and electrical measurements. Mechanical measurements usually include adhesion testing of the bond type, where an average detachment force is being determined from a statistical set of bonded chips. Heat transfer, mainly conduction in the case of LEDs, is usually measured on analogous electrical circuit with desired structures as an observed thermal resistor. As mentioned earlier especially the heat transfer of HPLEDs is crucial to determine in order to optimize the heat removal out of the QW area. Furthermore, electrical conductivity of the bond joint is also under interest and for example the minimum breakdown voltage is important to know. Alike chip attachment, also wire-bonding can be characterized in terms of mechanics, *e.g.*, pull test for the bonded wire, thermodynamics, *e.g.*, contact breakdown temperature, and electric power, *e.g.*, maximum current carrying capacity of the wire.

Apart from encapsulated LEDs, many measurements can be performed for the encapsulation material itself, such as refractive index or spectral transmission measurements. At least visual inspection is required for encapsulated LEDs to observe possible voids, cracks or impartial polymerization. All of these will reduce the light

extraction together with the natural absorbance of the used encapsulation material.

The packaging process as a whole can also be characterized with viable metrics. The process efficiency of a developed patch manufacturing process is usually measured with production quality and yield, *i.e.*, the percentage of successful end-products produced in comparison to the initial production potential. In industry, yield rates are carefully concealed secrets, because they determine the overall reproducibility and commercial profitability of the production line. The maximum reproducibility and as-high-as-possible yield are thus the core metrics to achieve. Usually these are achieved with standardization of optimum work steps, quality control, sufficient tool maintenance, extensive process flow and error monitoring and reporting. These were also the goals of this process development project. In addition to the before-mentioned production process implementation schemes, nowadays the so called just-in-time (JIT) manufacturing paradigm is widely used in commodity production industry, accentuating constant improvement, rigorously exact quality control, cleanliness, transparency, collaboration of vendors, careful cost monitoring and minimization of waste and stocks. For instance, in the case of LED production, the lower quality LEDs are usually still sold onwards but just on lower price.

## 4.2 Transmission of Epoxy

Three different epoxies were tested in respect to their optical transmission. The tested epoxies are designed especially for optical device and LED encapsulation and were acquired from an experienced epoxy manufacturer. The test samples were prepared by mixing the epoxy components and by dispensing the mixed epoxies into a cylindrical-shape silicone mold with the diameter and the depth of 1.5 cm and 0.5 cm, respectively. After curing, the solid epoxy piece was detached from the mold. Due to surface tension of the liquid epoxy, the casting resulted in an epoxy cylinder with an uneven back-side. Additionally some small air bubbles were observed on the surface. In order to smooth the uneven and air-bubble-containing surface, it was mechanically grind with an abrasive rotating plate and polished with a polishing paste. Also, a slightly differing surface treatments were applied to the sample set consisting of the same type of epoxy.

One epoxy sample was subjected to elevated temperatures in order to see the effect of temperature on the epoxy. The sample was placed on a hot plate and kept for 1-10 minutes at 300 °C. As a result, an optical degradation as a hint of yellow discoloration was observed. It was also noted that the slightly different surface treatments caused only minor variation on the spectral transparencies especially near the UV regime.

The optical transmission and absorption properties of the epoxy samples were measured by using a setup depicted schematically in figure 23. In this setup the used wide-spectrum light source was a high power incandescent lamp with focusing mechanical shutter. The focused propagating light went through the epoxy cylinder and then through a non-dispersive optical filter to adjust the light intensity and then the light entered the detector module. The incident light was collected with an integrating sphere connected with an optical fiber to a spectrometer. The spectrometer utilizes a prism to disperse different wavelengths of the incident light to a charge coupled device (CCD) sensor. The control software of the spectrometer analyzed automatically the measured data.

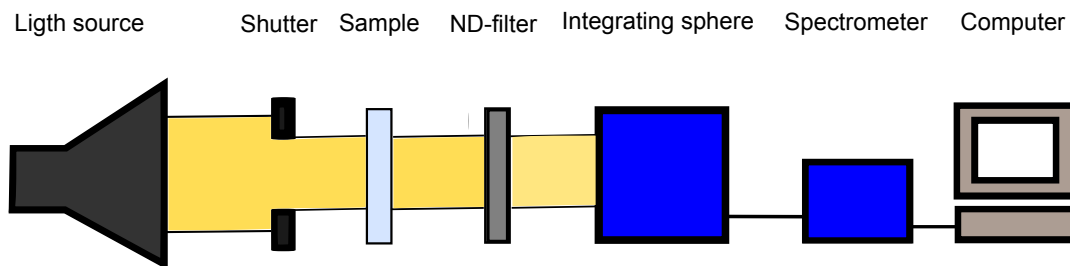


Figure 23: Transmission measurement setup for epoxy samples.

The transmission of the epoxy was obtained by comparing measured light spectrum with and without the epoxy sample in the incident light path. In this manner, the difference between the spectra were obtained by simply subtracting the corresponding data points from each others.

### 4.3 Electroluminescent Absolute Irradiance

As a part of the processing quality control, the EL spectra of the LEDs were studied as a function of the location on the processed SQW LED wafer. The EL properties of the LEDs were measured before and after the encapsulation, in order to test the effect of the encapsulation. In addition, the uniformity of the sample wafers devoted for this process development was characterized by measuring EL from a few carefully chosen places, shown in figure 24. For these tests, seven LED chips were back-end processed from three, approximately 1 cm x 1 cm, wafer areas.

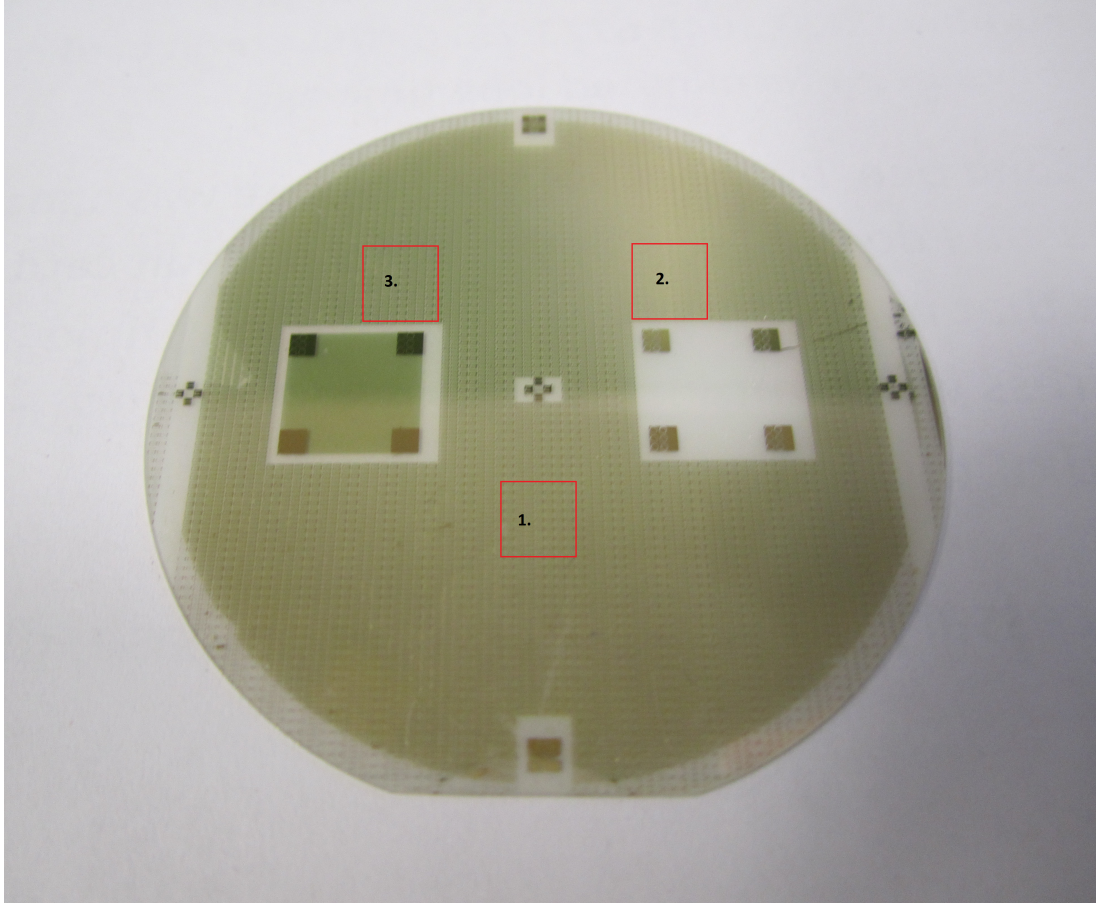


Figure 24: Three packaging test sites from a front-end processed SQW LED wafer illustrated. Each test site area, from which the back-end processed chips were chosen, were approximately 1 cm x 1 cm.

In the EL measurement setup, individual, encapsulated or non-encapsulated LED components were DC biased with a 20 mA current. The current was injected using a laboratory power source, which can measure voltage while injecting precisely defined current. Thus, the electrical performance of the LED under measurement could be constantly observed. The similar measurement setup was used in the EL measurement as in the transmission measurement. The integrating sphere was placed upon

the biased LED upside down in order to minimize the effect of ambient lighting. The same spectrometer as in the transmission measurement was used for measuring the light gathered by the integrating sphere. The control software of the spectrometer was then used for data analysis.

The spectrometer control software is capable to exclude the effect of the ambient lighting by comparing the measured ambient light, called the dark spectrum, to the actual measurement. In order to further minimize the effect of the dark spectrum, it was measured every time the measurement parameters were varied. Also, the measurements were averaged in order to minimize the noise levels. Due to these actions the absolute photon flux, peak wavelength, spectral width of the peak and the optical output-power values could be reliably measured. In the case of few samples also a power series was measured by regularly increasing the current and measuring the incident electrical power together with the EL metrics. From this data wall-plug efficiency (WPE) and EQE values as a function of drive current could be obtained.

## 5 Results

The spectral transparency, the photon flux, optical power and the central wavelength of the individual LEDs were measured using the measurement setups described in section 4. The results were used for further performance and quality analysis.

### 5.1 Transmittance of Epoxy

Transmittance of three different epoxy samples were measured with the setup described in section 4. Only slight deviations on the absorption characteristics were observed and thus, only the chosen epoxy is studied here in more detailed fashion. Figure 25 shows the measured transmittance with the raw data and the statistically corrected spectra. Figure 26 shows the spectral absorbance characteristics of the chosen epoxy when normalized to a path length of 1 cm.

The blue lines of the graphs include all the raw measurement points and exhibit major fluctuations but those flatten out when the measurement is averaged. The red lines are smoothed by averaging 50 moving data points from the raw data. The increasing fluctuation of both curves at the low energy end occurs because the CCD sensitivity diminishes at the limit of the visible regime.

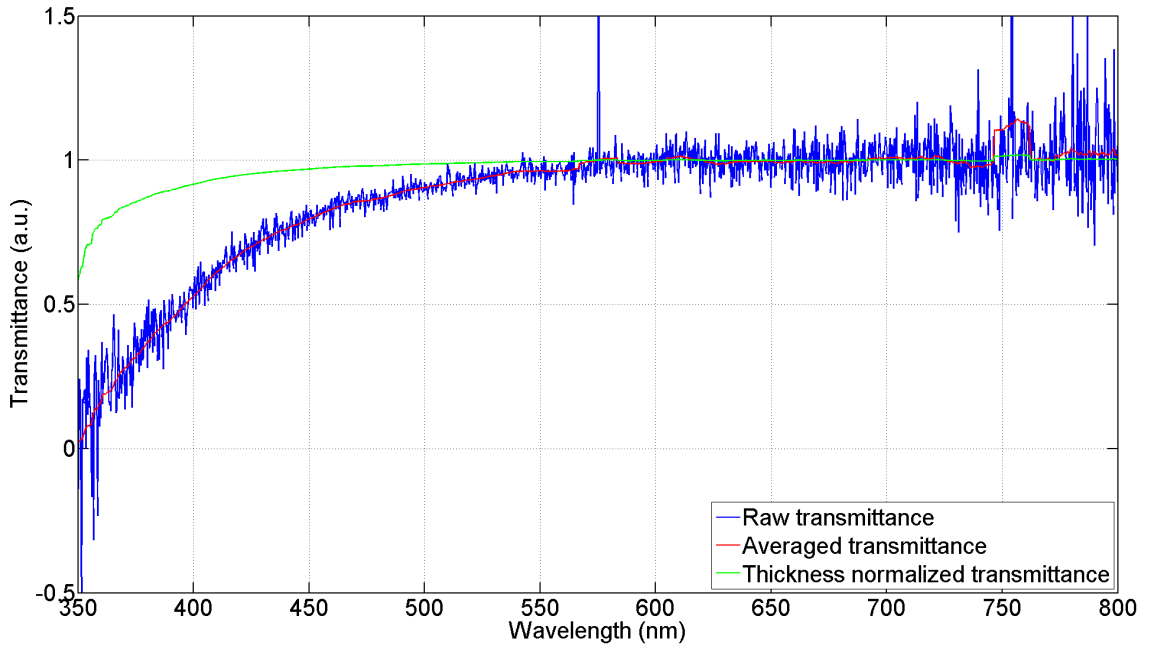


Figure 25: Transmittance of epoxy 301-2FL.

The manufacturer of the epoxy in question stated that the spectral transmission should be over 99% on the range of 400-1000 nm. However, it is unknown how the stated spectral transmission value of the technical data sheet is produced. Still, the

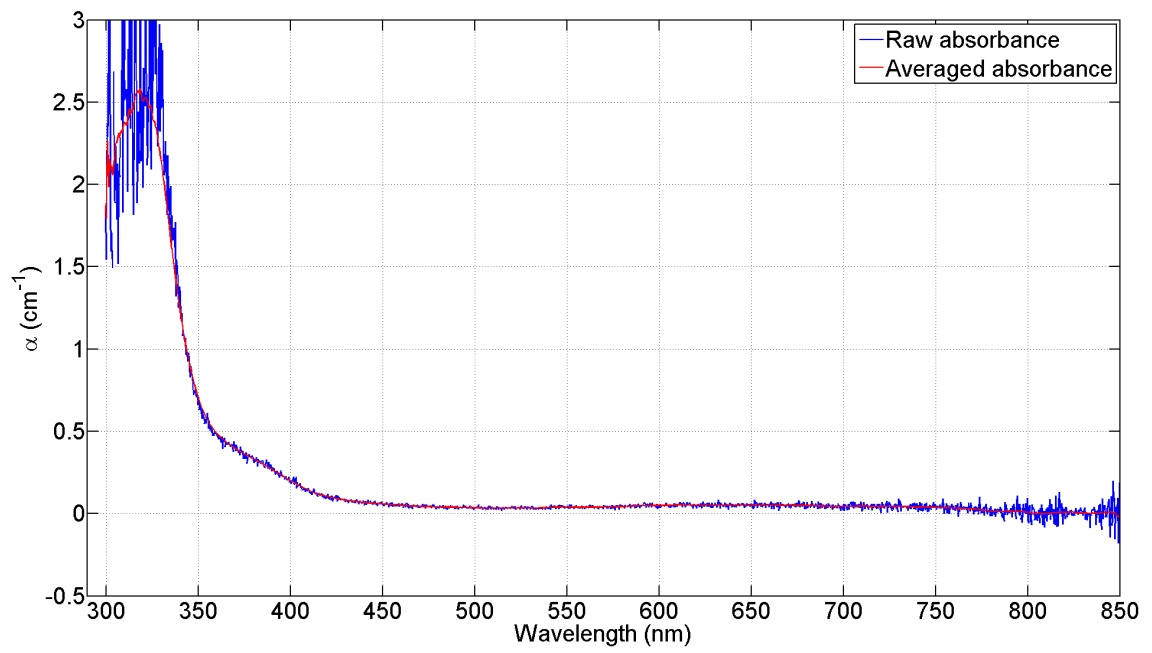


Figure 26: Absorbance spectrum of the epoxy. Illustrates spectral attenuation of light in a 1 cm travel distance in the epoxy.



absorbance and transmittance curve analysis shows that the transmission starts to drop approximately from 450 nm. At the low energy end the transmission stays on high level. The observed spectral transmission difference can be partially explained with natural light intensity attenuation inside the medium and partially on sample treatment induced defects. For instance, the epoxy samples had to be subjected to polishing treatments to produce as clear and flat surfaces as possible. It seems that the absorption in the epoxy and the internal reflections on the interfaces affect especially the high energy end of the transmission. Despite these results, the epoxy was expected to be applicable for the 450 nm LEDs of this work.

## 5.2 EL Performance

According to the presented absolute irradiance measurements, the optical power values and central emission wavelengths of 21 LEDs on three different wafer locations (see figure 24) before and after the encapsulation were measured and these results are illustrated in table 5. There were large differences between the encapsulation yields of the three wafer areas. Unfortunately only few samples were operational after the encapsulation from the areas 2 and 3. Still, on the area 1 the yield stayed high despite the encapsulation step and also other encapsulated LED sample sets demonstrated high yields on the encapsulation process and on the back-end process in general. One possible reason for unoperational samples might be the degraded quality of the contact metallization, because the samples from areas 2 and 3 had to wait quite long time for the epoxy encapsulation after the first EL measurement.

Furthermore, it was observed that the optical power of the encapsulated LEDs on all areas decreased by one third from the non-encapsulated ones. These are somewhat surprising results because epoxy encapsulation should function as an index matching interface between GaN and air and, thus, promote light extraction from the GaN. One explanation for these results could be the in-epoxy absorption on the emission wavelength of 450 nm. Indeed, as the results on the previous chapter showed, the transmission properties of the epoxy resin are not anymore at high level at the operation wavelength of the processed blue LEDs and could lead to the observed photon flux losses. In addition to the material attenuation in the material, fabrication related issues play a role. For instance, it is probable that small air bubbles formed inside the epoxy dome during the hardening, introducing further light power losses in the LED component. Furthermore, the chip location on the header, chip size and dome shape of the measured LEDs were not accurately optimized for ideal light extraction.

Table 5: Measured LED performance on three different wafer areas depicted in figure 24.

Parameter/LED-wafer location	Area 1	Area 2	Area 3	All
Avg. optical power pre-encap (mW)	4,05	2,40	2,25	3,00
Avg. optical power post-encap (mW)	2,05	2,00	1,60	2,05
Standard deviation (mW)	0,52	0,80	1,19	0,83
Emission peak pre-encap (nm)	448,8	455,5	450,7	451,7
Emission peak post-encap (nm)	448,4	451	450	450
Avg. EQE post-encap (%)	3,69	2,53	2,84	3,21

In addition to the optical power values from the absolute irradiance measurements, also the central emission peak was observed from the spectral shapes. These values varied slightly between different wafer locations as can be seen in table 5. Also, the

standard deviation (unbiased sample variance as an estimator) of all the samples (including before and after encapsulation) was 0,83 mW, which marks quite a sizable power value spread for a single LED wafer. One possible reason for these on wafer wavelength and output power variations can be found on the MOVPE QW growth step, where minor deposition deviations, connected to, *e.g.*, non-uniform gas flows or temperatures, could have caused this. Still the full-width-of-half-maximum was around 25 nm on every sample proving stable LED pulse distribution on the wafer.

Also, the EQE and WPE were calculated from the measured data. First, WPE was calculated by dividing the output optical power on the measured input electrical power per LED. The EQE was then obtained by dividing the WPE on the electrical efficiency of the LED. The electrical efficiency was calculated by dividing the photon energy with the measured operating voltage of an individual LED. Figure 27 shows the measured and calculated EQE and WPE of an end-packaged LED with respect to the drive current. The shapes of the plotted efficiency curves are typical for LEDs; EQE and WPE are exponentially decreasing when the drive current is increased.

The measured EQE and WPE values were quite modest in comparison to similar commercial low-power blue LEDs which can produce EQEs around 35%. Perhaps the biggest reason for weak performance can be found in the fact that the packaged LEDs were SQW-LEDs, which produce significantly less light than MQW-LEDs that are used in commercial products. Also, the light extraction from the QW was unoptimized due to the absence of mirroring backside of the chips and the reflective cup around the chip. In addition, the large chip size compared to the active chip area functioned as an unnecessarily large absorption mass for the produced light.

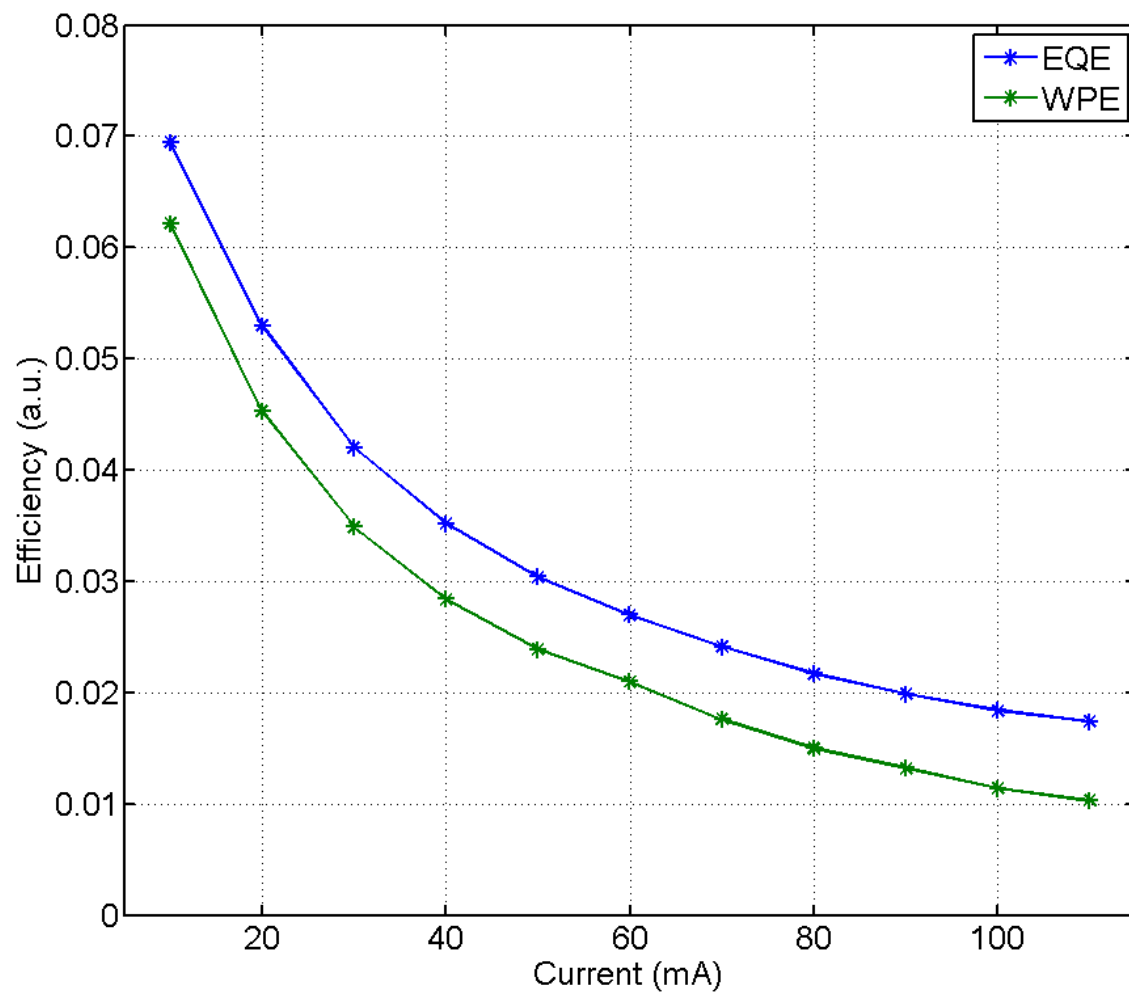


Figure 27: EQE and WPE of a packaged SQW-LED as a function of drive current.

## 6 Conclusion

In this thesis, a back-end process from processed wafer to encapsulated LED components was developed. The thesis includes a literature overview and description of the four main process steps: wafer dicing, chip bonding, wire-bonding and transparent encapsulation. As a result, packaged LEDs were produced and characterized. Furthermore, the performance of the processed LEDs was characterized by transmittance measurements of the encapsulation material and by EL measurements. All of the required tools for testing, characterization, front- and back-end fabrication are located at Aalto University's Micronova laboratory infrastructure. The front-end processed LED sample wafers used in this thesis comprised on SQW-LEDs of blue wavelength (450 nm) and were fabricated with MOVPE by Optoelectronics group.

The developed packaging process started from the singulation of chips from the sapphire wafer by a mechanical dicing machine. It was resolved that the critical dicing parameters to produce high yields included utilization of a 150- $\mu\text{m}$ -thick resin-bonded blade, feed rate of 0.3 mm/s, spindle speed of 12 RPM and dual-through-cut dicing mode. After the protective resist removal, the LED chip was bonded on its package. The package was a metallic two-pin header TO-46. The chip-to-header bonding process was done by two-component conducting epoxy. Dosing was controlled with timed dispenser setup after which the positioning of the LED chips was performed manually by using tweezers. The consecutive wire bonding process was optimized using manual wedge-wedge type bonder with an aluminum wire having a diameter of 25  $\mu\text{m}$ . The final process step was encapsulation with a transparent epoxy. For this purpose a 5-mm-dome LED silicone mold array stage was manufactured and used. The encapsulation of the LED components was done with transmission tested optical epoxy.

The experimental section of this thesis included performance measurements of the previously described back-end processed LEDs and the transmission of the optical epoxy samples. The spectral transmission measurements showed high-level transparency (over 95 %) of the chosen encapsulation epoxy at the LED emission peak wavelength of 450 nm. The transmission properties of the epoxy started to drop at shorter wavelengths. The EL performance characterization of the end-packaged LEDs included absolute irradiance measurements with an integrating sphere and a CCD detector unit. These measurements enabled the determination of the peak wavelengths of the LEDs together with the optical output and electrical input powers. LED performance describing EQE and WPE values were then calculated from this data.

The optical performance analysis was divided into two cases. First, the performance properties of LEDs at three different wafer locations before and after encapsulation were examined. It was found that the maximum averaged peak emission wavelength difference between the samples of the three areas was around 7 nm peak center being between 448-455 nm. For pre- and post-encapsulated LEDs the averaged optical

output powers differed significantly, ranging from 2,25 mW to 4,05 mW, respectively. This can be, at least partially, explained by optical power losses in the encapsulation epoxy. Some samples also featured air bubbles in the epoxy dome, which could further increase the absorption.

The second case of the performance analysis consisted of EQE and WPE power series measurements to demonstrate the effect of different drive current levels on the light output efficiency. The EQE-current curve complied with a typical LED performance, being exponentially decreasing as a function of current. The EQE values were lower than those of the commercial LEDs but this is not surprising for this kind of elementary-level packaging process. Still, at the typical 20 mA drive current the EQE of back-end processed LEDs was 5.3 % and the optical power 3 mW, which can be considered to be adequate for research purposes on the basis of clear visual luminance and high enough efficiency.

The goal of this thesis work was to develop a simple packaging process for LEDs operating in the visible regime for research purposes. Based on the completed detailed process flow documentation, extensive LED back-end processing literature overview, in-house manufactured processing tools, encouraging optical and electrical characteristics, and finally repeatable high yield process results, it can be stated that the developed process was successful. Nonetheless, there is a lot of room for improvement such as a possible white light LED production by incorporation of a phosphor to the encapsulation epoxy. Moreover, adoption of flip-chip assembly together with optimized chip size could provide major improvements to the performance metrics.

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## Appendix A

The set-up procedure and operation of the dicing saw are extensively documented in Micronova and are thus only briefly described here.

The dicing process should be started by turning on the curing oven to 50 °C for adhesion strengthening of the attachment between the tape and the wafer. Then, the wafer holder is built by tensing the blue tape in between of the two plastic rims on special pressing device. After that, the wafer is attached in the middle of the tape-rim combination by putting it top-side up on a clean room paper and then pressing carefully the tape side to provide tight and air-bubble-free contact with the wafer back-side. This combination should then be cured at 50 °C for 15 min.

The dicing machine preparation is a multistage process. First, the rotary vacuum pump need to be switched on, followed by the opening of the air line valve and the water tap for rinsing water jet. Then, the main power switch can be turned on together with the microscope monitor display. After that, the wafer chuck platform made from brass needs to be fasten on top of the fixed cylindrical flow line sub-mount. Next, the blade and its flange component need to be stacked and fastened on the sawing spindle. Once the blade is fully attached, the protective blade shield and rinse water pipeline combination need to be fastened by screws. Then the plastic cover should be lowered on top of the whole dicing stage area.

Next step is to choose, or determine, a correct dicing recipe through the user interface. If the recipe is predetermined it can be simply chosen from the list of recipes. If not, then the approximate values need to be defined. The developed dicing recipe for 2 inch LED-sapphire wafers is described in Table 2. After that, the spindle can be turned on and the blade together with incident high pressure water rinse starts. Next step is to choose the height sense in order to calibrate the blade to dicing plane distance. It can change over time due to the wear degree of blade and should be recalibrated for every wafer.

Then, the wafer-on-tape rim can be placed in the middle of the brass chuck and vacuum clamped. Next, the wafer need to be aligned with a microscope at first by bringing the microscope on top of the wafer with motorized position control and then focusing it on the surface of the wafer. In the case of a typical 2 inch LED-sapphire wafer, both of the microscopes can not be used for an typical alignment focusing due to a too long distance between the two microscope cameras. Thus, the alignment need be done with only one microscope by finding two patterns that are in parallel on the wafer surface and then by fixing one position cursor on one of those line-shapes and then comparing that to the corresponding line-shape on the other location. Then, the offset between these two pattern lines can be corrected with motorized rotation functionality of the substrate holder. When the alignment has been done the wafer needs to be moved to the initial cut position. The edge quality of the dicing street and its exact location on the monitoring screen can only

be determined after the first cut, so in the case of an important sample one should do the first cut to a dummy wafer.

The dicing process is initiated by choosing the cut-single or cut-auto mode. In case of the cut-auto the amount of cuts are predetermined on the dicing recipe and dicer will dice index-step determined sizes of chips and the chuck will turn 90 degree to achieve that. On the cut-single option, the dicer will perform only one cut. This is a good option if the dicing quality need to be monitored or if only few cut pieces are desired. When the dicing is done, the machine should be shut-down in the opposite order than when starting. The diced wafer on tape-rim can be separated from brass mount after releasing the vacuum clamp by lifting the whole brass-mount stage off and then carefully detaching them by hand or by using the pressure flow stage.

## Appendix B



### EPO-TEK<sup>®</sup> H20E Technical Data Sheet For Reference Only Electrically Conductive, Silver Epoxy

Number of Components:	<u>Two</u>	<u>Frozen Syringe</u>	Minimum Bond Line Cure Schedule*:	
Mix Ratio By Weight:	1:1		175°C	45 Seconds
Specific Gravity:		2.67	150°C	5 Minutes
Part A	2.03		120°C	15 Minutes
Part B	3.07		100°C	2 Hours
Pot Life:	2.5 Days		80°C	3 Hours
Shelf Life:	One year at 23°C	One year at -40°C		

*Note: Container(s) should be kept closed when not in use. For filled systems, mix contents of each container (A & B) thoroughly before mixing the two together. \*Please see Applications Note available on our website.*

#### Product Description:

EPO-TEK<sup>®</sup> H20E is a two component, 100% solids silver-filled epoxy system designed specifically for chip bonding in microelectronic and optoelectronic applications. It is also used extensively for thermal management applications due to its high thermal conductivity. It has proven itself to be extremely reliable over many years of service and is still the conductive adhesive of choice for new applications. Also available in a single component frozen syringe.

#### EPO-TEK<sup>®</sup> H20E Advantages & Application Notes:

- Processing info: It can be applied by many dispensing, stamping and screen printing techniques.
  - Dispensing: compatible with pressure/time delivery, auger screws, fluid jetting and G27 needles, in a single-component fashion.
  - Screen Printing: best using >200 metal mesh, with polymer squeegee blade with 80D hardness.
  - Stamping: small dots 6 mil in diameter can be realized.
- Misc / Other notes
  - Many technical papers written over 30-40 year lifetime. Contact [techserv@epotek.com](mailto:techserv@epotek.com).
  - Over 1 trillion chips attached at a single company: no failures, Six Sigma and Certified Parts Supplier award winner.
  - Versatility in curing techniques including box oven, SMT style tunnel oven, heater gun, hot plate, IR, convection, or inductor coil.
  - Many custom modified products available, for the following improvements: viscosity and appearance, flexibility and thermal conductivity. Contact [techserv@epotek.com](mailto:techserv@epotek.com) for your best recommendation.

**Typical Properties:** (To be used as a guide only, not as a specification. Data below is not guaranteed. Different batches, conditions and applications yield differing results; Cure condition: 150°C/1 hour; \*denotes test on lot acceptance basis)

#### Physical Properties:

\*Color: Part A: Silver Part B: Silver  
 \*Consistency: Smooth, thixotropic paste  
 \*Viscosity (@ 100 RPM/23°C): 2,200 – 3,200 cPs  
 Thixotropic Index: 4.63  
 \*Glass Transition Temp.(Tg): ≥ 80°C (Dynamic Cure  
 20–200°C /ISO 25 Min; Ramp -10–200°C @ 20°C/Min)  
 Coefficient of Thermal Expansion (CTE):  
 Below Tg:  $31 \times 10^{-6}$  in/in/°C  
 Above Tg:  $158 \times 10^{-6}$  in/in/°C  
 Shore D Hardness: 75  
 Lap Shear Strength @ 23°C: 1,475 psi  
 Die Shear Strength @ 23°C: > 5 Kg / 1,700 psi  
 Degradation Temp. (TGA): 425°C

#### Weight Loss:

@ 200°C: 0.59%  
 @ 250°C: 1.09%  
 @ 300°C: 1.67%

#### Operating Temp:

Continuous: -55°C to 200°C  
 Intermittent: -55°C to 300°C

#### Storage Modulus @ 23°C: 808,700 psi

Ions: Cl<sup>-</sup> 73 ppm

Na<sup>+</sup> 2 ppm

NH<sub>4</sub><sup>+</sup> 98 ppm

K<sup>+</sup> 3 ppm

\*Particle Size: ≤ 45 Microns

#### Electrical Properties:

\*Volume Resistivity @ 23°C: ≤ 0.0004 Ohm-cm

#### Thermal Properties:

Thermal Conductivity: 2.5 W/mK  
 Based on standard method: Laser Flash  
 Thermal Conductivity: 29 W/mK  
 Based on Thermal Resistance Data:  $R = L \times K^{-1} \times A^{-1}$

#### Thermal Resistance: (Junction to Case)

TO-18 package with nickel-gold metallized 20 x 20 mil  
 chips and bonded with EPO-TEK<sup>®</sup> H20E (2 mils thick)  
 EPO-TEK<sup>®</sup> H20E: 6.7 to 7.0°C/W  
 Solder: 4.0 to 5.0°C/W

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## EPO-TEK<sup>®</sup> H20E Suggested Applications

- **Semiconductor IC Packaging**
  - Die-attaching chips to leadframes; compatible with Si and MEM's chips, 260°C lead-free reflow and JEDEC Level I packaging requirements.
  - Capable of being snap cured in-line, as well as traditional box oven techniques.
  - Adhesive for solderless flip chip packaging and ultra fine pitch SMD printing.
- **Hybrid Micro-electronics**
  - A comparable alternative to solder and eutectic die attach, in terms of thermal performance; very commonly no more than 1-2°C/watt difference in thermal resistance.
  - Die-attaching of quartz crystal oscillators (QCO) to the Au posts of TO-can style lead-frame.
  - Used with GaAs chips for microwave/radar applications up to 77GHz.
  - SMD attach adhesive which can be cured simultaneously with die-attach processes.
    - Compatible with Au, Ag, Ag-Pd terminations of capacitors and resistor SMDs.
  - NASA approved low outgassing adhesive.
  - Adhesive for EMI and Rf shielding of Rf, microwave and IR devices.
- **Electronic & PCB Circuit Assembly**
  - Used to make electrical contacts in acoustical applications of speakers/microphones.
  - Electrical connection of piezo's to PCB. Pads of PZT are connected to many kinds of circuits using H20E, including ink jet heads, MEMs and ultrasound devices.
  - Automotive applications include pressure sensing and accelerometer circuits.
  - Electrically conductive adhesive (ECA) for connections of circuits to Cu coils in Rf antenna applications such as smart cards and RFID tags.
  - ECA for attaching SMDs to membrane switch flex circuits. Compatible with Ag-PTF and carbon graphite PCB pads. A low temperature "solder free" solution.
  - Solar-Photovoltaic industry
    - ECA for the electrical connection of transparent conductive oxide (TCO) to PCB pads.
    - Replacement of solder joints of Cu/Sn ribbon wire, from cell-to-cell; a common "solar cell stringing" adhesive.
    - Die-attach of III-V semiconductor chips to substrates used in solar concentrator technology, such as CdTe and GaAs.
    - An effective heat-sink on thermal substrates using Cu, BeO, aluminum nitride, etc.
    - Ability to be dispensed in high volumes via dots, arrays, and writing methods.
- **Medical Applications**
  - USP Class VI adhesive for circuits requiring implantation/biocompatibility.
  - Die-attaching photo diode arrays in X-ray circuits.
  - Vibration resistant adhesive for ultrasound applications < 20 MHz frequency; making the electrical connection of PZT to Au/PCB substrate.
  - Electrical connections of die, SMDs and QCO for pacemaker hybrid circuits.
  - A common ECA for hearing aid applications using hybrid, ECM or MEMs technology.
- **Opto-Electronic Packaging Applications**
  - Adhesive for fiber optic components using DIP, Butterfly or custom hybrid IC packages. As an ECA, it attaches waveguides, die bonds laser diodes and heat sinks the high power laser circuits.
  - Die-attaching IR-detector chips onto PCBs or TO-can style headers.
  - Die-attaching LED chips to substrates using single chip packages, or arrays.
    - Adhesion to Ag, Au and Cu plated leadframes and PCBs.
  - Electrical connection of ITO to PCBs found in LCD industry.
    - A low temp ECA for OLED displays and organically printable electronics.

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## Appendix C

Process flow for the developed chip attachment to TO-46 headers. The numerical order of the list refers to the process steps illustrated in figure 18.

1. Setup preparation: the used metal headers should be attached to a holder and cleaned with IPA in order to achieve stable and successful bonding conditions. Also the chip pickers should be cleaned. The dispensing device is prepared by first opening the main gas valve, thus providing air pressure, and then switching it on and choosing or determining the dispensing recipe.
2. Mixing of bond epoxy: the mix ratio by weight for H20E is 1:1 and the mixing can be performed for instance with a toothpick. The epoxy used in this process is not sensitive to small deviations in mix ratio, but care is nevertheless required.
3. Dispensing setup preparation: the syringe of pressurized dispenser is loaded with the mixed epoxy. This can be done by two means. Either by sucking the epoxy in through the needle or by taking the piston out on the air pressure side of the material chamber and dosing the epoxy in. The first method is time consuming but the wasted epoxy is minimized. The latter one, on the contrary, permits dosing of larger amounts faster but wastage is larger. After loading the epoxy in the needle, the plastic piston should be brought into the contact with the epoxy mass in controllable fashion and then the needle need to be attached to the pressure air line of the dispensing device.
4. Dispensing of the bond epoxy: this is done by first determining the proper time at a certain output pressure in which the desired volume of epoxy is dispensed out of the needle. A small epoxy amount can be achieved in around 0.5 s pressure time and at a pressure of 8 bar. When the proper pressure and time parameters have been found, dispensing can be started by bringing the needle in the vicinity of the metal header and doing the dosing by pressing the air pressure controlling foot pedal.
5. Chip placement: after dispensing the epoxy, the LED chips are picked carefully with tweezers and pressed firmly against the bond epoxy area.
6. Curing: an oven annealing in temperature of 120 °C and consecutive time of 15 minutes can be used for the chip-headers. Also longer (shorter) times with, consecutive, lower (higher) curing temperatures can be used due to the exponential nature of the bonding reaction.

## Appendix D

Wedge-wedge wire-bonding process for LEDs.

1. Setup preparation: the first step is to position the attached LED and header combination onto a stable holder and to place that exactly perpendicular with respect to the bond needle. The required stability was achieved by using two-sided tape to attach the sample mounting stage (which was FR-4 plate based bond platform) to the backside of the component. The LED-component pins can be pushed through the tape covering the pin-holes. Before further positioning, it is advisable to check that the wire actually comes out through the via of the bond needle and, if not, the wire should be fed through the cavity of the needle by using precision lock tweezers. After the LED components are mounted to the sample holder, it can be placed on top of the metal rim spacer, which instead is on the x-y-precision stage.
2. Wire bonder preparation: in the next step, the LED components need to be well illuminated with the spot lights of the wire bonder and observed through the microscope to obtain the optimal positioning and focus spot. Then the proper bond recipe should be chosen through the user interface. The process optimized recipes are presented in Tables 3 and 4.
3. Initiation of bond process: the first actual step of bond process itself is to press the bond-button of the controller while the destination chip bondpad is in the middle of the microscope view. As a consequence, the needle descends to the first workheight where it is high above the chip but should still be visible in the microscope. The next bond command further brings the needle down to a searchheight, which is in a close proximity of the first bond pad. From there, one needs to do a precision adjustments by
  - (a) rotating the LED-component holder so that the end-destination bond pad is parallel with respect to the needle (in this case *i.e.*, the uplifted pin-plane of the TO-46);
  - (b) bringing the needle as close as possible to the chip surface with manual height control (*i.e.*, rolling the controller wheel), even so that the dangling wire end touches the surface of the chip;
  - (c) moving the wire-needle combination directly above the bond pad, while the needle is still pinning the wire against the chip pad. It might be that in this point even more height control is needed.
4. Bonding: when the bond needle with the pinned wire is in the middle of the bond pad of the chip, the actual bonding can be performed. Then, the wire is pressed with the predetermined bondweight under US against the pad and hopefully a successful bond is formed. As a result of that, the clamp holding the wire above the needle will open and the needle itself will ascend to the first loopheight, as depicted in figure 20 (d).

5. Wire looping and the destination bond: from the first loopheight, the bond-stage should be now directly moved towards the user of the bonder by moving the controller mouse towards oneself. When it seems that the needle with the fed wire is quite close to the end-pad, another bond needs to be made, thus lowering the needle to loopheight 2. From there it is more easier to determine the height from the end-pad and the needle can be moved effortlessly on top of it. Once there, the needle needs to be brought to the searchheight 2, where the exact y-axis location can be honed together with the needle-wire-combination height but with strict tolerances because the wire feeding clamp is now closed. Then, the last bond needs to be done according to the destination bond recipe. If the recipe was successful, the wire will be cut to the recipe-determined tail length and the needle will return to workheight.
6. The bond of the second contact: this can be implemented in the same way as the first bond described in steps 3 to 5. However, it should be noted that the destination bond in this case is under the chip plane and that is why there is a greater need of wire and ineptness to provide that will easily result in wire contacting the edge of the chip and possibly in a short-circuit. Also, one should direct the second wire always away from the first one, in order to minimize the risk of contact between the wires and parasitic capacitance between them.

In the case of an unsuccessful bond or other issue one should home the needle, thus returning the needle to the highest position and to exit the recipe view from the user interface.



# Appendix E



## ELASTOSIL® M 4601 A/B

RTV-2 Silicone Rubber / Mold Making

### Characteristics

Pourable, addition-curing, two-component silicone rubber that vulcanizes at room temperature.

### Special characteristics

- Very good flow
- Fast and non-shrink cure at room temperature which can be accelerated considerably by the application of heat
- Low hardness (Shore A approx. 28)
- High tear strength
- Excellent long-term stability of the mechanical properties of the vulcanizate
- Outstanding resistance to common casting resins

### Application

Due to the outstanding resistance to casting resins as well as the superior mechanical properties, ELASTOSIL® M 4601 A/B is especially suitable for all molds of models with extensive undercuts that are to be reproduced in casting resins.

As a low-Shore addition-curing RTV-2 silicone rubber that cures without undergoing dimensional shrinkage, ELASTOSIL® M 4601 A/B is also extremely suitable for casting all other common reproduction materials, particularly if absolutely accurate copies of models with pronounced undercuts are required.

### Product data (uncured)

Property	Test method	Unit	Value	
Component			A	B
Color			White	Reddish brown
Density at 23 °C		[g/cm³]	1.14	1.01
Viscosity at 23 °C, after stirring	ISO 3219	[mPa s]	15,000	800

### Product data (catalyzed A + B)

Property	Test method	Unit	Value
Mixing ratio	A : B	[pbw]	9 : 1
Viscosity at 23 °C	ISO 3219	[mPa s]	10,000
Pot life (up to 60,000 mPas)		[min]	90
Curing time, tack-free		[h]	12

### Product data (cured)

Property	Test method	Unit	Value
Color			Reddish brown
Density at 23 °C in Water	ISO 2781	[g/cm³]	1.13
Hardness Shore A	ISO 868		28
Tensile strength	ISO 37	[N/mm²]	6.5
Elongation at break	ISO 37	[%]	700
Tear strength	ASTM D 624 B	[N/mm]	> 30
Linear shrinkage		[%]	< 0.1

After 24 h at 23 °C.

These figures are intended as a guide and should not be used in preparing specifications.



## Processing

### Important

The platinum catalyst is contained in component B.

### Caution

Only components A and B with the **same lot number** may be processed together!

Comprehensive instructions are given in our leaflet "Wacker RTV-2 Silicone Rubber - Processing."

Detailed information on other mold-making compounds in the ELASTOSIL® M range is contained in our brochure "ELASTOSIL® M. Mold-Making Compounds For Maximum Precision".

## Storage

ELASTOSIL® M 4601 A/B should be stored between 5 °C and 30 °C in the tightly closed original container. The 'Best use before end' date of each batch appears on the product label.

Storage beyond the date specified on the label does not necessarily mean that the product is no longer usable. In this case however, the properties required for the intended use must be checked for quality assurance reasons.

## Safety information

Components A and B of the addition-curing grade ELASTOSIL® M 4601 contain only constituents that over many years have proved to be neither toxic nor aggressive. Special handling precautions are therefore not required, i.e., only the general industrial hygiene regulations apply.

Detailed safety information is contained in each Material Safety Data Sheet, which can be obtained from our sales offices.

## Additional information

Please visit our website [www.wacker.com](http://www.wacker.com)

The data presented in this leaflet are in accordance with the present state of our knowledge, but do not absolve the user from carefully checking all supplies immediately on receipt. We reserve the right to alter product constants within the scope of technical progress or new developments. The recommendations made in this leaflet should be checked by preliminary trials because of conditions during processing over which we have no control, especially where other companies' raw materials are also being used. The recommendations do not absolve the user from the obligation of investigating the possibility of infringement of third parties' rights and, if necessary, clarifying the position. Recommendations for use do not constitute a warranty, either express or implied, of the fitness or suitability of the products for a particular purpose.

The management system has been certified according to DIN EN ISO 9001 and DIN EN ISO 14001



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Version 7.00 from 27-08-07 replaces  
Version 6.00 from 11-04-07

For technical, quality, or product safety questions, please contact:

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## Appendix F

Silicone LED-component casting mold fabrication process.

1. Setup preparation: the mold piece consists of commercial LED lamps attached on a FR-4 sample stage which is guided through three threaded rods to obtain a controlled contact with the mold cavity. The attachment of LEDs to the FR-4 stage can be done by two-sided tape. It is very important that all the pieces are clean in order to avoid undue contamination of the silicone.
2. Mixing of silicone components: silicone components A and B need to be mixed in 9:1 weight ratio in a glass or plastic cup. At least 1 deciliter of silicone should be mixed in order to fully fill the mold volume of the pre-described molding stage.
3. Bubble removal: the mixed silicone is usually full of air bubbles and those need to be removed. This can be done by placing the silicone on a desiccator and vacuum pumping it. After around two minutes of vacuum pumping it can be assumed that the vacuum level is high enough and the silicone can be removed from the desiccator. Usually the air bubbles arise to the surface of the liquid and need to be mechanically punctured to get rid of them. To achieve a decent level of silicone uniformity, usually at least three vacuum treatments are required.
4. Dispensing of silicone: the air-bubble-free silicone can be poured to the mold volume. The volume of this mold stage ought to be filled very near to the fullest even though the transferable LED-domes displace the liquid silicone surface slightly. If it seems that after the pouring there still are air bubbles present, one should subject the whole molding stage with the silicone to the needed vacuum treatments.
5. The molding: next, the prepared mold stage, holding the mold component LEDs, is brought carefully down to the liquid silicone by sliding it down through the threaded rods. Using the stage fixed to the rods and the nuts around the rods as an adjustment scheme it is possible to accurately bring the commercial LED models to contact with the liquid silicone. With this scheme it is possible to control the height of the desired dome shape. In order to provide a fully stable molding condition, the mold stage can also be fixed from above with the nuts.
6. Hardening and finishing: the liquid silicone is fully hardened in 24 hours at room temperature (23 °C). After that, the molding stage needs to be carefully lifted up, occurring usually so that the model LEDs are detached from the two-sided tape and are left in their silicone pockets. Then the LEDs can be shaken individually to get them detached from the silicone pocket walls. Finally, they can be easily lifted off, leaving behind LED-encapsulation-ready silicone mold.

## Appendix G



### EPO-TEK® 301-2FL

#### Technical Data Sheet

For Reference Only  
Low Stress, Optical Epoxy

Number of Components: Two  
Mix Ratio By Weight: 100:35  
Specific Gravity:

Part A 1.06  
Part B 0.89

Pot Life: 10 Hours

Shelf Life: One year at room temperature.

*Note: Container(s) should be kept closed when not in use. \*Please see Applications Note available on our website.*

*—IF PART A CRYSTALLIZES IN STORAGE, PLACE CONTAINER IN A WARM OVEN UNTIL CRYSTALLIZATION DISAPPEARS. ALLOW TO COOL TO ROOM TEMPERATURE BEFORE MIXING WITH THE PART B HARDENER. \*Please refer to Tech Tip #7 on our website. —*

Minimum Bond Line Cure Schedule\*:  
80°C 3 Hours  
23°C 3 Days

#### Product Description:

EPO-TEK® 301-2FL is a two component optical, medical, and semiconductor grade epoxy resin. It is a more flexible version of EPO-TEK® 301-2.

#### EPO-TEK® 301-2FL Advantages & Application Notes:

- Suggested for LCD optical lamination and sealing of glass plates. The product can resist yellowing over 17 days of continuous UV light exposure. Suitable for LED encapsulation.
- Ease of use: potting and casting, encapsulation, and adhesive.
- Semiconductor applications: underfill for flip chips, glob top encapsulation over wire bonds, spin coating at wafer level.
- Compliant adhesive that will be resistant to impact or vibrations. Low stress adhesive for bonding optics inside OEM / scientific instruments.
- Fiber optic adhesive; bundling fibers, terminating fiber into ferrule, adhesive for mounting optics inside fiber components, bonding glass cover slip over V-groove; spectral transmission of visible and IR light.
- BIOCOMPATIBLE and NON-TOXIC; complies with USP Class VI biocompatibility standards for medical devices and implantation applications.
- Adhesion to glass, quartz, metals, wood and most plastics is very good.
- May also be used for impregnating wooden or porous objects for artifact restoration.
- Capable of both heat cure and room temperature cure.

**Typical Properties:** *(To be used as a guide only, not as a specification. Data below is not guaranteed. Different batches, conditions and applications yield differing results; Cure condition: 80°C/3 Hours ; \*denotes test on lot acceptance basis)*

Physical Properties:	
*Color: Part A: Clear/Colorless Part B: Clear/Colorless	Weight Loss:
*Consistency: Pourable Liquid	@ 200°C: 0.50%
*Viscosity (@ 100 RPM/23°C): 100 – 200 cPs	@ 250°C: 0.96%
Thixotropic Index: N/A	@ 300°C: 3.52%
*Glass Transition Temp.(Tg): ≥ 45°C (Dynamic Cure 20—200°C /ISO 25 Min; Ramp -10—200°C @ 20°C/Min)	Operating Temp:
Coefficient of Thermal Expansion (CTE):	Continuous: - 55°C to 150°C
Below Tg: 56 x 10 <sup>-6</sup> in/in/°C	Intermittent: - 55°C to 250°C
Above Tg: 211 x 10 <sup>-6</sup> in/in/°C	Storage Modulus @ 23°C: 152,946 psi
Shore D Hardness: 70	Ions: Cl <sup>-</sup> 105 ppm
Lap Shear Strength @ 23°C: > 2,000 psi	Na <sup>+</sup> 58 ppm
Die Shear Strength @ 23°C: ≥ 10 Kg / 3,400 psi	NH <sub>4</sub> <sup>+</sup> 8 ppm
Degradation Temp. (TGA): 325°C	K <sup>+</sup> 19 ppm
	Particle Size: N/A
Optical Properties @ 23°C:	
Refractive Index @ 23°C (uncured): 1.5115 @ 589 nm	Spectral Transmission: > 97% @ 1000 – 1600 nm
	> 99% @ 400 – 1000 nm
Electrical & Thermal Properties:	
Thermal Conductivity: N/A	Volume Resistivity: ≥ 0.6 x 10 <sup>12</sup> Ohm-cm
Dielectric Constant (1 KHz): 3.54	Dissipation Factor (1 KHz): 0.013

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## Appendix H

Transparent epoxy molding process description for LEDs.

1. Encapsulation device and sample preparation: first, the semi-packaged LEDs are fixed to the holder stage (FR-4 template) by two sided, thick, tape strips. The tapes provide necessary elevation to a proper mold-to-component contact. Prior to the chip-on-header attachment the tape should be perforated through the correct pin holes in order to avoid misalignment of the epoxy domes and the LED component area. The correct holes on the FR-4 template are marked on the opposite side of the stage by green color. In addition, the whole encapsulation device and the mold holes especially should be cleaned carefully.
2. Epoxy mixing and dispensing: epoxy components A and B need to be mixed in 100:35 weight ratio in a glass or plastic cup. Mold holes require only minor amounts of epoxy, but in order to obtain a proper handling of the material, one ought to mix around 5 ml of liquid. Next, the epoxy requires usually few vacuum treatments, equivalent to silicone mold molding. Once the epoxy is bubble free, it can be carefully sucked into a pipette and then dispensed on the silicone mold holes. While filling the holes, one should be careful not to under fill them because that will result in improper or totally lacking attachment. Over fill, on the contrary, is not that critical because the spilled epoxy will usually form a 'necklace' to the LED component and it can be broken apart easily.
3. Encapsulation stage stacking and hardening: after dispensing epoxy the upper (components holding) stage is brought down through the threaded rods so that the LED components and the holder tape are in full contact with the mold level silicone. To guarantee that the contact is air tight, the upper stage should be pressed against the lower part by fixing it with nuts. After that the epoxy needs to be harden at room temperature for 3 days.
4. Encapsulated LED-component detachment: after hardening, the mounted stages can be separated by carefully and evenly rolling the three lifting nuts under the top-stage. The encapsulated LEDs will either come off with the upper stage or then detach from it, thus leaving in their silicone pockets. Either way, the encapsulated components can now be easily picked up. In the case of misalignment of the components at the step 1, partial encapsulation as represented in figure 22 d) may occur.